"A MODIFIED THREE STAGE COMPARATOR USING DYNAMIC COMPARATOR WITH HIGH SPEED"

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ABSTRACT

A three-stage comparator and its modified version is to improve the speed and reduce the power dissipation. When compared with conventional comparators that is, traditional two-stage comparator, this proposed comparator will enhance additional amplification structure, with this the efficiency of the proposed model will increase enormously. Two stage comparator uses pMOS input pair whose hole mobility is less which limits the regeneration speed. The three- stage comparator makes it possible to use nMOS input pairs in both the regeneration stage and the amplification stage, further increasing the speed. It has high hole mobility which increases speed compared to the two stage comparator. Furthermore, in the proposed modified version of three-stage comparator, a CMOS input pair is adopted at the amplification stage. It also adds an extra signal path in the regeneration stage, which helps increase the speed further. But its power dissipation is high. By replacing the pre-amplifier stage with dynamic comparator which helps in enhancing the speed.

Keywords: Comparator, High Speed, Power, CMOS, pMOS, nMOS

INTRODUCTION

A dynamic comparator is a component used in electronic circuits to compare two voltages or signals and produce an output based on their relative values. They are commonly used in applications such as analog-to-digital converters, where precise voltage comparison is required. It typically operates in a static mode. It employs dynamic operation, where it charges and discharges internal nodes to speed up the comparison process. Dynamic operation involves actively controlling the charging and discharging of internal nodes to improve speed and reduce power consumption. This is achieved by utilizing techniques such as precharging, where internal nodes are initially charged to a certain voltage level before the comparison process begins. During comparison, these charged nodes are discharged and recharged based on the input signals.

LITERATURE SURVEY

[1] H. Zhuang, W. Cao, X. Peng, and H. Tang, "A Three-Stage Comparator and It's Modified Version With Fast Speed and Low Kickback," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., May 2021. A three-stage comparator is a fundamental building block in analog circuit design, commonly used in applications like analog-to-digital converters (ADCs), voltage regulators, and oscillators. It compares two input voltages and produces a digital output indicating which input is larger. The basic structure typically consists of three stages: input stage, amplifier stage, and output stage. Input stage is responsible for sensing the input voltages and providing them to the amplifier stage. Amplifier stage amplifies the voltage difference between the inputs provided by the input stage. Output stage generates the digital output based on the amplified voltage difference. [2] K. Krishna, and N. Nambath, "Cascode Cross-Coupled Stage High-Speed Dynamic Comparator in 65nm CMOS," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 31, no. 7, Jul. 2023. A cascode cross-coupled stage consists of two pairs of transistors connected in a "cross-coupled" manner, typically using complementary pairs to ensure symmetric operation. This configuration offers advantages like increased speed, reduced sensitivity to process variations, and improved

stability. It's particularly useful in applications requiring fast and accurate comparisons of analog signals. [3] A. Khorami, and Md. Sharifkhani, "A Low-Power High-Speed Comparator for Precise Applications," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 2018. In contrast to the conventional comparator a PMOS latch is used in the latch which is activated with a predetermined delay during the evaluation phase. At this stage the cross coupled circuit increases the differential voltage slowly and reduces the common mode voltage to provide a strong drive for the input PMOS latch stage. In the proposed circuit, the delay of the evaluation phase is long enough to achieve the minimum required preamplification gain. If the preamplifier and the latch work in different time slot the power consumption is improved. The cross coupled circuit increases the differential voltage mainly when the preamplifier is turned off and enhances the speed however the main purpose is to reduce the input common mode voltage of the latch.

EXISTING METHOD

The modified version of three stage comparators typically incorporate additional features to meet specific needs such as low power consumption, faster response times, or better noise immunity. A modified version of a three-stage comparator could involve changes in the amplification stages or the addition of features like further improve in speed. It consists of CMOS input pair at first stage pre - amplifier. Modified three stage comparator consists of enhanced per-amplification stage. These modifications enhance the comparators performance in specific applications, whether they need to handle low-power scenarios, operate in a noisy environment, or respond more rapidly to changes in the input signal.

In order to further improve the speed, this brief proposes a modified version of three-stage comparator. Compared to the three stage comparator in the previous section, the only difference is that the modified version has the extra first two stages and extra paths M 29–32 in the latch stage. The extra paths M29–32 apply extra signal onto the latching nodes OUTP and OUTN, thus the regeneration speed is increased further, and the input referred offset and noise are suppressed further.

In the reset phase, CLK is 0 and CLKB is 1. The RP1 and RN1 in Fig 1(c) are reset to GND, while FP1 and FN1 are reset to *V*DD. This turns off M30 and M32 in Fig 1(c), ensuring that there is no static current in the extra path M29–32.

In the amplification phase, CLK rises to 1 and CLKB falls to 0. RP1 and RN1 in Fig 1(c) rise to *V*DD (R stands for rise). Then, FP1 and FN1 fall to GND (F stands for fall). Because the rising of RP1 and RN1 occurs before the falling of FP1 and FN1, the extra paths in Fig 1(c) are turned on for a limited time, drawing a differential current from the latching nodes OUTP and OUTN. This generates a differential voltage at OUTP and OUTN, which helps speedup the regeneration phase afterward and suppress the comparator input referred offset and noise. After FP1 and FN1 fall to GND, the extra paths in Fig 1(c) are turned off again to prevent the static current.

Overall, the modified version of three-stage comparator has the advantages of faster speed, lower input referred offset and noise, and lower kickback noise. It is suitable for high-speed high-resolution SAR ADCs.

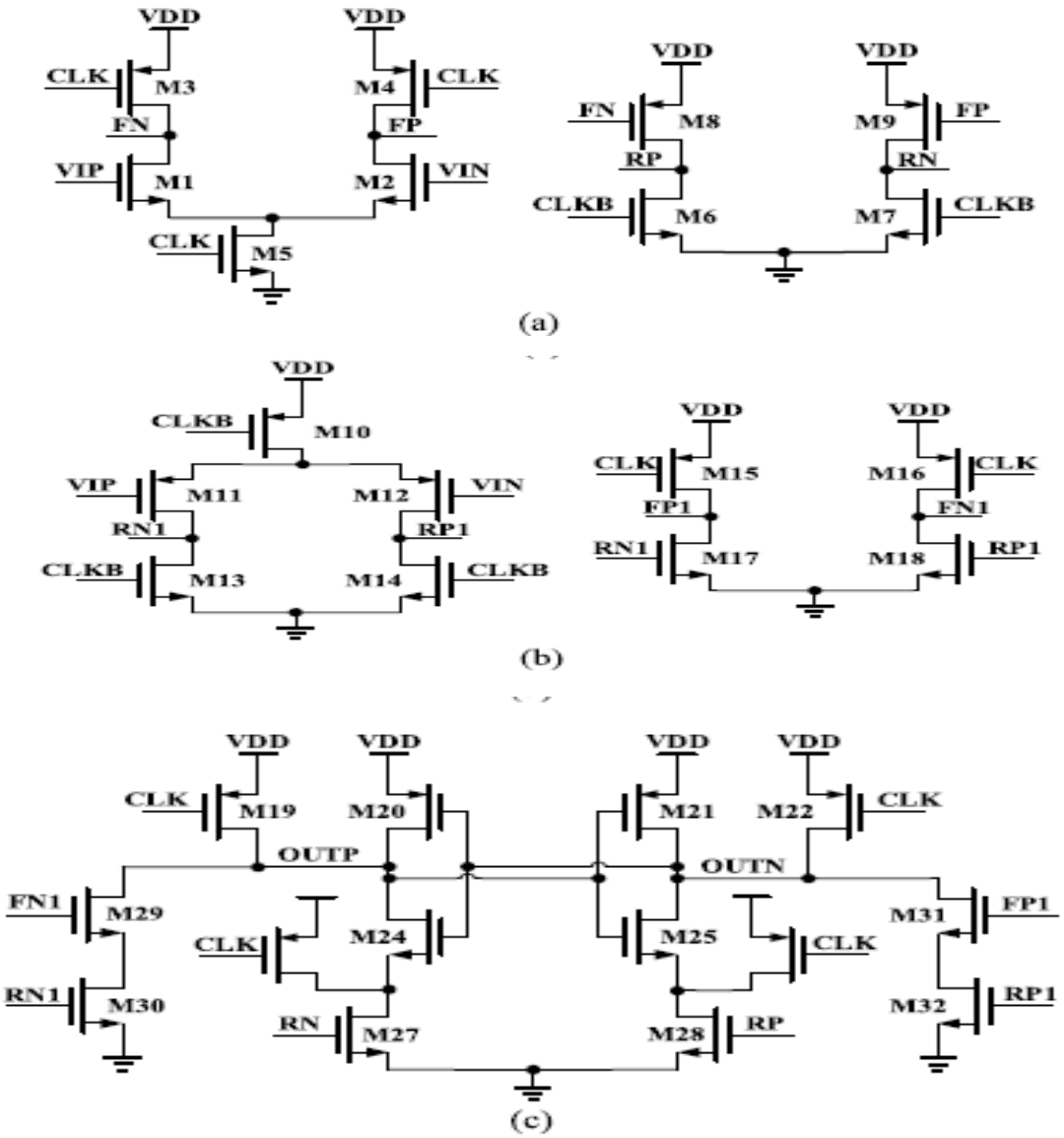


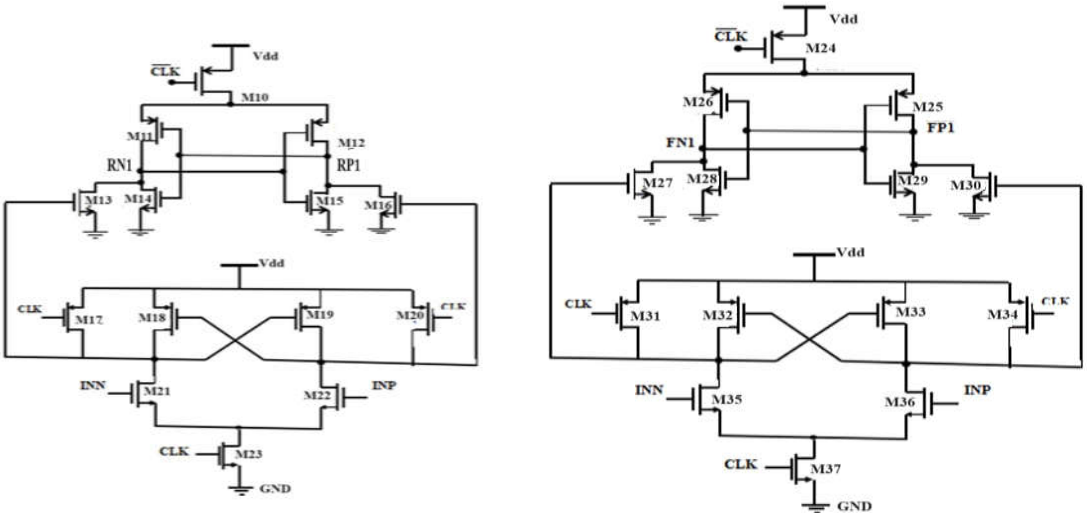
Fig 1: Modified version of three-stage comparator. (a) Original first two stages (preamplifiers) with nMOS input pair. (b) Extra first two stages (preamplifiers) with pMOS input pair. (c) Third stage (latch stage).

PROPOSED METHOD

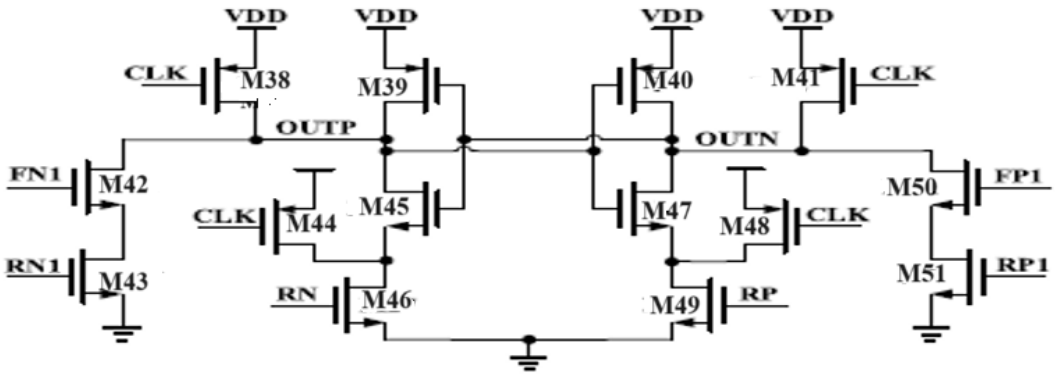
Preamplifier stage amplifies the input signals to a suitable level for comparison. The clock signal initiates the charging of the dynamic nodes. In Latching stage the comparator compares the voltages on the dynamic nodes. When one node charges faster than the other, it indicates which input is greater. The clock signal then latches the output based on this comparison result. Output stage provides the final output of the comparator, which is typically a digital signal indicating the relationship between the two input voltages (e.g., which is greater). Clock Signal's Role: The clock signal ensures that the comparison process occurs at the right Time and synchronizes the operation of different stages within the comparator. It's crucial for the proper functioning of the dynamic comparator. In summary, the modified three-stage comparator using a dynamic comparator operates by amplifying input signals, comparing them dynamically, and generating an output based on the comparison result, all synchronized with a clock signal.

MODIFIED THREE STAGE USING DYNAMIC COMPARATOR ARCHITECTURE

In order to further improve the speed, this brief proposes a modified three-stage comparator using Dynamic comparator. Compared to the Modified three stage comparator in the previous section, the only difference is that Dynamic comparator is introduced in place of one of the preamplification stages of modified three stage comparator.



(b)



(c)

Fig 2: Modified Three stage Comparator using Dynamic Comparator(a) Original first two

stages (preamplifiers) (b) Dynamic comparators (c) Third stage (latch stage).

In the reset phase, CLK is 0 and CLKB is 1. The RP1 and RN1 are reset to GND, while FP1 and FN1 are reset to VDD. This turns off M43 and M51, ensuring that there is no static current in the extra path M42, M43, M50 and M51.

In the amplification phase, CLK rises to 1 and CLKB falls to 0. RP1 and RN1 rise to VDD (R stands for rise). Then, FP1 and FN1 fall to GND (F stands for fall). If the voltage at VIP is high and VIN is low, this generates differential volage at OUTP. If the voltage at VIP is low and VIN is high, then this generates differential voltage at OUTN. which helps speedup the regeneration phase afterward and suppress the comparator input referred offset and noise. After FP1 and FN1 fall to GND, the extra paths are turned off again to prevent the static current.

Overall, this modified three stage using dynamic comparator enhances the speed, power dissipation and efficiency.

RESULT ANALYSIS

The schematic circuits of the comparators discussed above are simulated in Mentor Graphics version Tanner tool 2022 using 50nm CMOS technology. The comparators are simulated with the supply voltage of 1V. The power, area and delay of the different comparators are compared for best utilization in ADC. In an ADC, dynamic comparator, high-speed comparator and low power comparator are popularly used in the circuit the implementation.

Implementation Process: Set up the simulation environment in Mentor Graphics, specifying the parameters of the comparator circuit. After defining input waveforms applied to the comparator inputs, Run the simulation in Mentor Graphics to observe the behaviour of the comparator over time. This will generate waveform data representing various signals in the circuit. Analyze the captured waveforms to understand the operation. Identify any improvements in terms of speed, accuracy, power consumption.

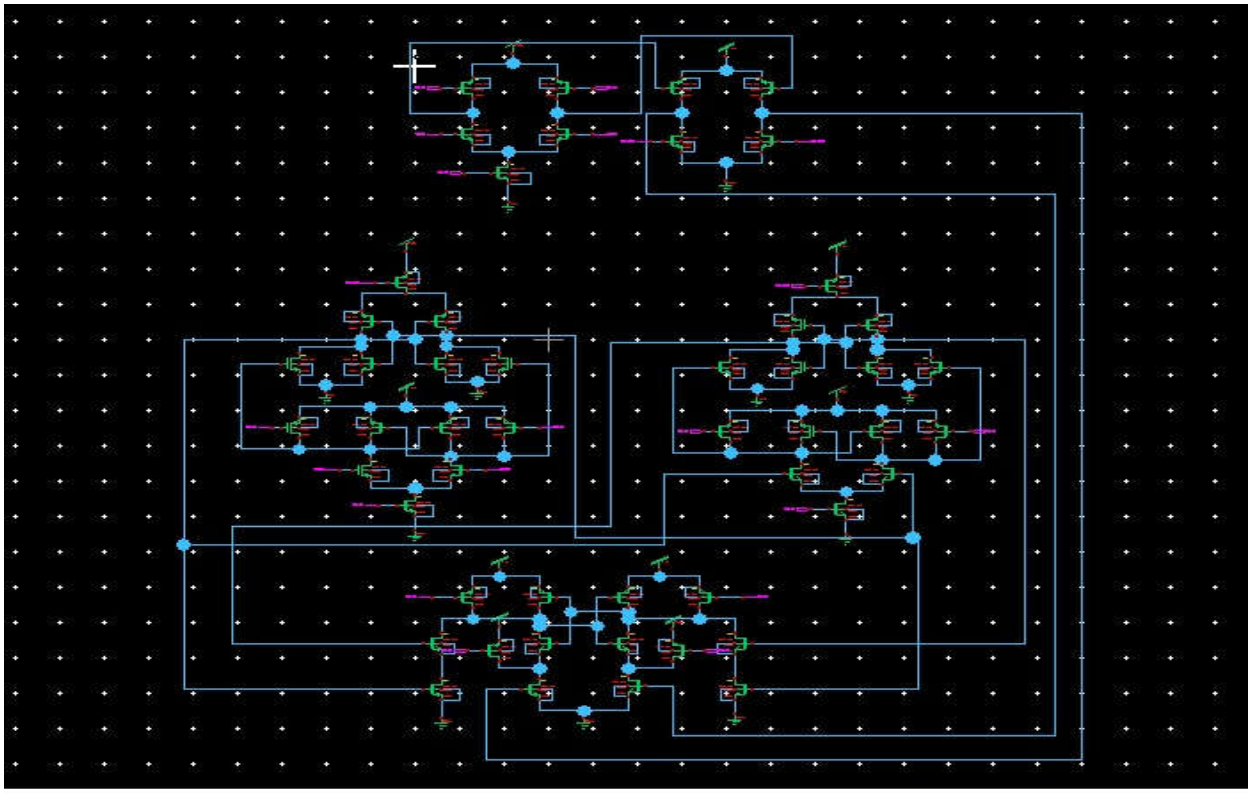


Fig 3: Schematic diagram of modified three stage comparator using dynamic comaparator

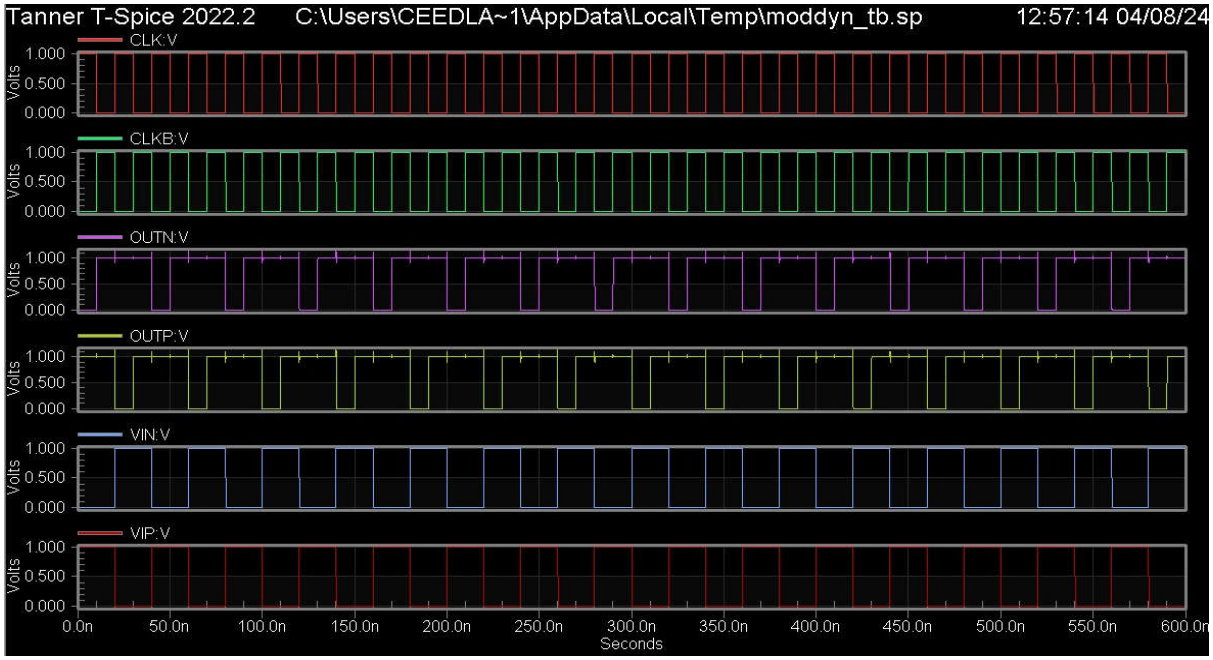


Fig 4: Output response of Modified three stage comparator using dynamic comparator

Waveform Explanation: When CLK is HIGH(Active) and Non inverting input (VIP) is HIGH whereas Inverting input (VIN) is LOW then OUTP is HIGH, OUTN is LOW. When Non inverting input is LOW and Inverting input is high then OUTP is LOW, OUTN is HIGH. When CLK is given LOW(Inactive) irrespective of the inputs the outputs OUTP and OUTN will be HIGH.

Table.1Performance comparision of comparators

Parameters	Three stage Comparator	Modified Three stage Comparator	Modified Three stage Comparator using Dynamic Comparator
Technology	50nm CMOS	50nm CMOS	50nm CMOS
Supply Voltage	1.2V	1.2V	1.2V
Input Signal range	1V	1V	1V
Delay	29.905ns	20.241ns	19.461ns
Number of Transistors	19	32	51
Power	0.01nW	0.0224nW	0.0186nW

CONCLUSION

In this paper, the design and analysis results of the comparators have been presented for CMOS ADC applications. The simulation results of the various CMOS comparators are obtained in Mentor Graphics version Tanner tool 2022 using 50nm technology and compared with each other for performance evaluation. In comparison, a Modified Three stage comparator using dynamic comparator has low propagation delay. Finally, measured results validate the effectiveness of these comparators. By carefully considering the specific design requirements and trade-offs, engineers can select the most suitable comparator architecture for their applications, balancing speed, noise, and power efficiency to meet performance goals.

REFERENCES

[1] H. Zhuang, W. Cao, X. Peng, and H. Tang, “A Three-Stage Comparator and It’s Modified Version With Fast Speed and Low Kickback,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., May 2021.

[2] K. Krishna, and N. Nambath, “Cascode Cross-Coupled Stage High-Speed Dynamic Comparator in 65nm CMOS,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 31, no. 7, Jul. 2023.

[3] A. Khorami, and Md. Sharifkhani, “A Low-Power High-Speed Comparator for Precise Applications,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 2018.

[4] P. Harpe, E. Cantatore, and A. van Roermund, “A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with data-driven noise reduction,” in Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, Feb. 2013, pp. 270–271.

[5] H. S. Bindra, C. E. Lokin, D. Schinkel, A.-J. Annema, and B. Nauta, “A 1.2-V dynamic bias latch-type comparator in 65-nm CMOS with 0.4-mV input noise,” IEEE J. Solid-State Circuits, vol. 53, no. 7, pp. 1902–1912, Jul. 2018.

[6] Y. T. Wang et al., “An 8-bit 150-MHz CMOS A/D converter,” IEEE J. Solid-State Circuits, vol. 35, no. 3, pp. 308–317, Mar. 2000.

[7] B. Razavi, “The StrongARM latch [A circuit for all Seasons],” IEEE Solid StateCircuits Mag., vol. 7, no. 2, pp. 12–17, Spring 2015.

[8] M. Abbas, Y. Furukawa, S. Komatsu, J. Y. Takahiro, and K. Asada, “Clocked comparator for

high-speed applications in 65nm technology," in Proc. IEEE Asian Solid-State Circuits Conf., Nov. 2010, pp. 1–4.
[9] J. Lu and J. Holleman, "A low-power high-precision comparator with time-domain bulk-tuned offset cancellation," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 60, no. 5, pp. 1158–1167, May 2013.
[10] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise selfcalibrating dynamic comparator for high-speed ADCs," in Proc. IEEE Asian Solid-State Circuits Conf., Nov. 2008, pp. 269–272.
[11] D. Shinkel et al., "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2007, pp. 314–315.
[12] M. van Elzakker et al., "A 10-bit charge-redistribution ADC consuming 1.9 μW at 1 MS/s," IEEE J. Solid-State Circuits, vol. 45, no. 5, pp. 1007–1015, May 2010. [13] M. Brandolini et al., "A 5 GS/s 150 mW 10 b SHA-less pipelined/SAR hybrid ADC for direct-sampling systems in 28 nm CMOS," IEEE J. Solid-State Circuits, vol. 50, no. 12, pp. 2922–2934, Dec. 2015.