# DESIGN AND IMPLEMENTATION OF 7T-SRAM CELL USING BODY BIAS CONTROLLER

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## ABSTRACT

Low power consumption of electronic devices has become one of the most desirable factors in the present day's technology. Static random access memory (SRAM) being an integral part of most of the electronic gadget suffers from leakage current which results in static power dissipation. This becomes crucial especially for those systems which are portable and have limited power supply. This work therefore proposes a body bias controller implemented with a 7T SRAM cell at 45 nm CMOS technology node which lowers the static power consumption. Moreover, it also reduces write delay due to reduction in threshold voltage of proposed design. It has been noticed that there is a reduction of 40%, 28%, 41.9% and 30% in static power dissipation of the proposed design when compared to 6T SRAM cell, 7T SRAM cell, respectively. The proposed design can thus be a suitable alternative for low power SRAMs.
So, an improved power dissipation and reduction of delay for proposed design will be implemented by using CMOS 45nm technology and Tannertools_v2022.2.

## INTRODUCTION

SRAM (Static Random Access Memory) is a type of semiconductor memory that is used in VLSI (Very Large-Scale Integration) chips to store data. The word "static" means that the memory retains its contents as long as the power is turned on. Random access means that locations in the memory can be written to or read from in any order, regardless of the memory location that was last accessed. An SRAM cell is the basic building block of SRAM memory and is made up of several transistors that can store one bit of data. An SRAM cell is able to communicate its data. This operation does not affect the data i.e., Read operation is non-destructive. The data of an SRAM cell can be set to any binary value regardless of its original in write operation. In order to store data at fast speeds without refresh cycles, SRAM, a vital component of digital circuitry, uses bistable latching mechanisms. Because of its flip-flop and transistor architecture, it can support ASICs and microprocessors with fast access times and strong data retention. To enhance memory subsystems and adjust to new trends in semiconductor design, engineers must have a thorough understanding of the nuances of SRAM.

## LITERATURE SURVEY

[1] Static Random-Access Memory cell is designed with two inverters, which are crosslinked like as latch form. This latch is made connection to two-bit line along with two transistors T1 and T2. Now both transistors are capable to alter their modes (open or close) under control of word line, and this entire process is controlled by address decoder. [3] When word line goes to ground level then both transistors get turned off, and latch starts to retain own state. Static RAM working is divided into three operations like as Read, Write and Hold [4] The design of a low power 6T SRAM

cell makes use of two cross coupled CMOS inverters. The circuit's primary benefit is its low static power dissipation, which is constrained by leakage current [13]. The current circuit has a high noise immunity due to its high noise margin. The read and write functions are enabled for the word lines. In order to turn the access transistors to the ON state, the SRAM cells are connected to the bit cells [20]. The read action does not destroy the data that is stored in the cell. This circuit is capable of running on a low voltage power source.

**EXISTING METHODS:**

## 1.Conventional 6T SRAM Cell:

Two cross-coupled CMOS inverters are used in the design of a low power 6T SRAM cell. Leakage current limits the circuit's minimal static power dissipation, which is its primary benefit [13]. High noise immunity is a feature of the current circuit due to its high noise margin. For the read and write operations, the word lines are turned on. The bit cells and SRAM cells are coupled in such a way that the access transistors are turned to the ON state [20]. The read procedure leaves the data that is stored in the cell undamaged. Low voltage power supplies can be used to run this circuit. When designing a memory cell SRAM, the CMOS circuits' inverters are connected back to back and given The final two basic access transistors at the end.
In the Fig. 1 above, SRAM is displayed.In the cross-coupled inverters, the nMOS function as pull-down transistors with a large current carrying capacity, the access transistors have a higher strength, and the pMOS function as pull-up transistors with a weaker capacity in order to achieve both read and write stability.The bit lines are linked to the N3 and N4 access transistors [9]. This circuit uses two inverter circuits that are linked together and connected crosswise, or cross coupled inverters. When the access transistors are connected to the write line and the write line value is 1, the access transistors are always in the ON state.The output terminals are the Q and Qbar.

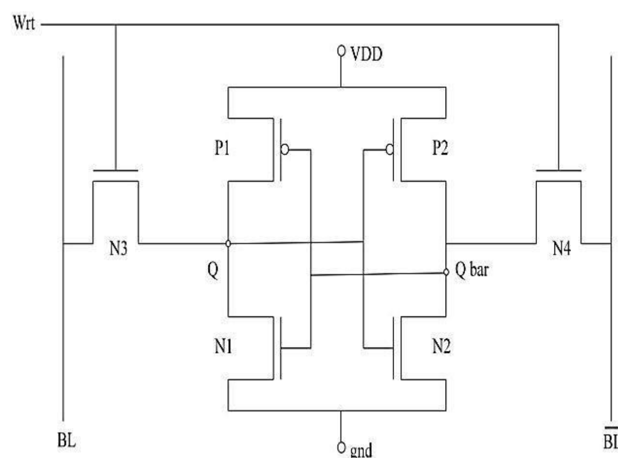


Figure.1. Schematic diagram of 6T Sram Cell

## 2. 7T SRAM Cell:

At 45 nm technology, an SRAM is implemented using the following techniques: The first method involves raising the NMOS transistors' Vth in SRAM cells. While increasing the Vth of drive NMOS transistors raises the logical threshold voltage of the CMOS inverter, increasing the Vth of access NMOS transistors keeps the Node V1 voltage from significantly reaching "0." The second method involves lowering the word-line (WL) voltage level at read operations from VDD. Due to PMOS cell leakage current, low Vdd read operations result in minimal storage destructions in SRAM cells, while write operations at lower Vdd levels are not possible. Utilizing a unique write mechanism, the other 7TSRAM cell lowers the activity factor of discharging the bit-line pair by relying only on one of the two bit-lines to complete a write operation. There is a minimum 49% write power savings, according to the simulation. Following careful cell transistor sizing, both read delay and static noise margin are preserved. One of the constraints was the space above the

standard 6T SRAM cell.

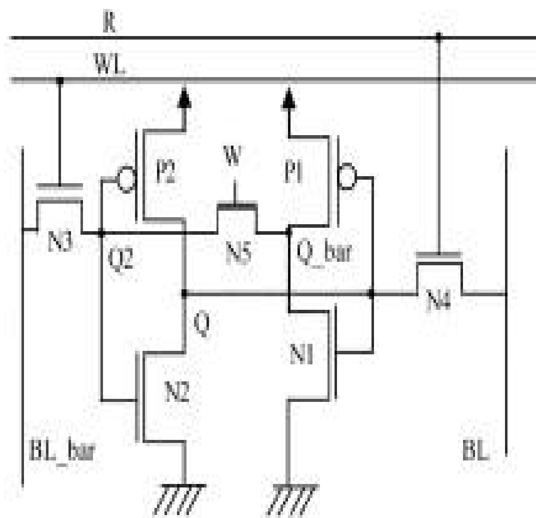


Figure.1. Schematic diagram of 7T Sram Cell

**PROPOSED METHOD**

The proposed body bias controller design, depicted in Figure 1, is pivotal for maintaining the stability and reliability of SRAM cells. It operates by utilizing NMOS diode loads (M1, M2, and M3) to create a voltage drop equivalent to three times the threshold voltage of individual NMOS transistors. This drop is crucial for regulating the body voltage within specified limits, which is essential for the proper functioning of SRAM cells. The controller's operation is governed by two primary input signals: Wen and Cntrl. Wen indicates write (high) or read/hold (low) operations, while Cntrl is used for periodic capacitor refreshing to prevent charge loss due to leakage. Key components, including transistors M4, PM1, and M5, play distinct roles in ensuring proper operation during different modes. Capacitor behavior facilitates voltage stability across its terminals, enabling the generation of positive and negative voltages at node Y depending on the operation mode. The waveform output and voltage limits are carefully managed to ensure compatibility with SRAM cell requirements. Additionally, the minimum VDD requirement is determined by specific output voltage objectives, considering both the controller and SRAM cell necessities. Achieving a balance between component design and operational requirements is crucial for maintaining stability across varying conditions, such as power supply voltage and temperature fluctuations. Overall, the design aims to provide consistent body bias voltages critical for SRAM cell stability, thereby ensuring reliability in integrated circuit operation.

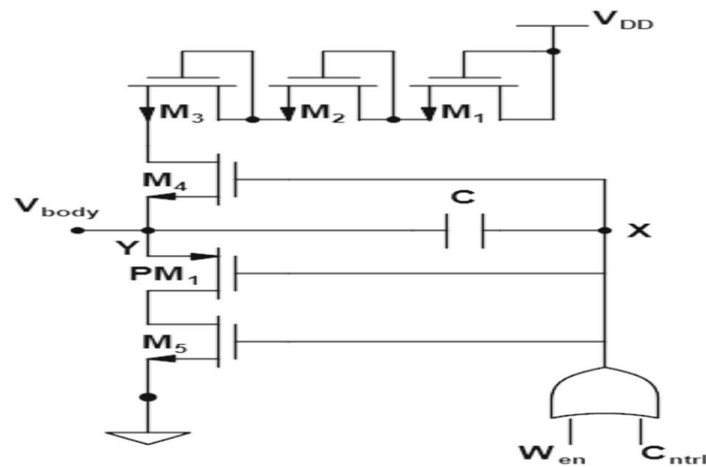


Figure.1. Schematic diagram for proposed model

**THE DESIGN STRUCTURE OF THE 7T SRAM USING BODY BIAS CONTROLLER**

The 7-transistor Static Random Access Memory (7T SRAM) cell is a specialized design used for specific applications that require a balance between performance, power consumption, and stability The Body bias is a technique used to dynamically adjust the threshold voltage (Vt) of a CMOS transistor , which allows a designer to tune a circuits behaviour to meet both the power and performance specifications.The proposed body bias controller design, depicted in Figure 1, is pivotal for maintaining the stability and reliability of SRAM cells. It operates by utilizing NMOS diode loads (M1, M2, and M3) to create a voltage drop equivalent to three times the threshold voltage of individual NMOS transistors. This drop is crucial for regulating the body voltage within specified limits, which is essential for the proper functioning of SRAM cells. The controller's operation is governed by two primary input signals: Wen and Cntrl. Wen indicates write (high) or read/hold (low) operations, while Cntrl is used for periodic capacitor refreshing to prevent charge loss due to leakage. Key components, including transistors M4, PM1, and M5, play distinct roles in ensuring proper operation during different modes. Capacitor behavior facilitates voltage stability across its terminals, enabling the generation of positive and negative voltages at node Y depending on the operation mode. The waveform output and voltage limits are carefully managed to ensure compatibility with SRAM cell requirements. Additionally, the minimum VDD requirement is determined by specific output voltage objectives, considering both the controller and SRAM cell necessities. Achieving a balance between component design and operational requirements is crucial for maintaining stability across varying conditions, such as power supply voltage and temperature fluctuations. Overall, the design aims to provide consistent body bias voltages critical for SRAM cell stability, thereby ensuring reliability in integrated circuit operation. There are some advantages of proposed controller: The output voltage levels can be adjusted by increasing or decreasing the number of NMOS diode loads. Thus, it can be used for various applications. The controller will eliminates the need of negative power supply for reverse biasing. The controller can be used to any design of SRAM cell like 6T, 7T , 8T, 9T ana 10T The SRAM cell

design consists of pull-down and access transistor.

**RESULT ANALYSIS**

The schematic circuits of the SRAMs discussed above are simulated in Tanner Tools using CMOS 45nm technology. The SRAM with BBC is simulated with the supply voltage of 1V. The power, area and delay of the different SRAMs are compared for best utilization in low power applications.

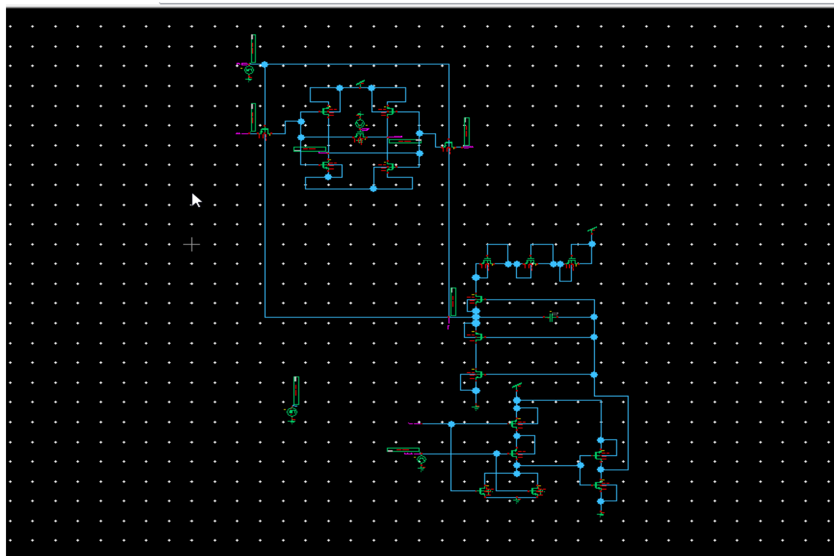

Fig.2. 7T SRAM Using Body Bias Controller

Table 1: Comparison of proposed work with other designs.

| Parameters | 6T SRAM | 7T SRAM | 7T WITH BBC |
|---|---|---|---|
| Technology | 45nm | 45nm | 45nm |
| Supply Voltage(V) | 1v | 1v | 1v |
| Total Delay(ns) | 110 | 92.8 | 49.13 |
| Total Power(nW) | 19.1 | 16.8 | 14.32 |

Table 1 shows the power and delay of the basic 6T and 7T SRAM and designed 7T SRAM with BBC by using Tanner tool of 45nm technology. The conventional 6T SRAM cell has the power of 19.1 and 7T SRAM cell has the power value of 16.8. The designed 7T SRAM cell with BBC power is reduced by 25% from basic 6T SRAM design. The conventional 6T SRAM cell has the delay of 110 ns and 7T SRAM cell has the delay value of 92.8ns and the designed 7T SRAM cell with BBC delay is reduced by 45% from basic 6T SRAM design.

## CONCLUSION

In this paper, a novel body bias controller is implemented with 7T SRAM cell for reducing power dissipation delay and total power. Furthermore, the proposed work can be designed at some advanced processes which results to enhance the capacity of memory that can be useful for high-performance networking applications. The proposed body bias controller (BBC) circuit implemented with a 7T SRAM cell is effective in reducing static power dissipation. By carefully controlling the electrical properties of the cell, we can make it work better, allowing for faster and more reliable operations in electronic devices like smartphones and computers.

## REFERENCES


1. Design and Analysis of SRAM cell using Body Bias Controller for Low Power Applications. *Circuits Syst Signal Process* 40, 2135–2158 (2021).
2. K.I. Agawa, H. Hara, T. Takayanagi, T. Kuroda, A bitline leakage compensation scheme for low-voltage SRAMs. IEEE J. Solid-State Circuits 36(5), 726–734 (2001).
3. M. Blagojevi´c, M. Cochet, B. Keller, P. Flatresse, A. Vladimirescu, B. Nikoli´c, A fast, flexible, positive and negative adaptive body-bias generator in 28 nm FDSOI, in 2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits), Honolulu, HI, pp. 1–2 (2016).
4. B.H. Calhoun, A.P. Chandrakasan, A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation. IEEE J. Solid-State Circuits 42(3), 680–688 (2007)
5. M.F. Chang, C.F. Chen, T.H. Chang, C.C. Shuai, Y.Y. Wang, Y.J. Chen, H. Yamauchi, A compact-area low-VDD min 6T SRAM with improvement in cell stability, read speed and write margin using a dual-split-control-assist scheme. IEEE J. Solid-State Circuits 52(9), 2498–2514 (2017).
6. L. Chang, D.M. Fried, J. Hergenrother, J.W. Sleight, R.H. Dennard, R.K. Montoye, L. Sekaric, S.J. McNab, A.W. Topol, C.D. Adams, K.W. Guarini, Stable SRAM cell design for the 32 nm node and beyond, in Digest of Technical Papers. 2005 Symposium on VLSI Technology, 2005, IEEE, pp. 128–129 (2005).
7. R.H. Dennard, F.H. Gaensslen, H.N. Yu, V.L. Rideout, E. Bassous, A.R. LeBlanc, Design of ionimplanted MOSFET's with very small physical dimensions. IEEE J. Solid-State Circuits 9(5), 256–268 (1974)
8. N. Kamae, A. Tsuchiya, H. Onodera, A body bias generator with low supply voltage for within-die variability compensation. IEICE Trans. Fundam. Electron. Commun. Comput. Sci. 97(3), 734–740 (2014)
9. S.M. Kang, Y. Leblebici, CMOS digital integrated circuit (Tata Macgraw-Hill education, New York, 2003)
10. C.I. Kumar, B. Anand, Design of highly reliable energy-efficient SEU tolerant 10T SRAM cell. Electron. Lett. 54(25), 1423–1424 (2018)
11. C.B. Kushwah, S.K. Vishvakarma, D. Dwivedi, Single-ended boost-less (SE-BL) 7T process tolerant SRAM design in sub-threshold regime for ultra-low-power applications. Circuits Syst. Signal Process. 35(2), 385–407 (2016)
12. Y.C. Lai, S.Y. Huang, X-calibration: a technique for combating excessive bitline leakage current in nanometer SRAM designs. IEEE J. Solid-State Circuits 43(9), 1964–1971 (2008)
13. R. Lorenzo, S. Chaudhury, A novel 9T SRAM architecture for low leakage and high performance. Analog Integr. Circ. Sig. Process 92(2), 315–325 (2017)
14. J.K. Mishra, H. Srivastava, P.K. Misra, M. Goswami, Analytical modeling and design of 9T SRAM cell with a leakage control technique. Analog Integr. Circ. Sig. Process 101(1), 31–43 (2019)

15. J.K. Mishra, H. Srivastava, P.K. Misra, M. Goswami, A 40 nm low power high stable SRAM cell using separate read port and sleep transistor methodology, in IEEE International Symposium on Smart Electronic Systems (iSES) (Formerly iNiS), Hyderabad, India (2018)
16. M. Moghaddam, S. Timarchi, M.H. Moaiyeri, M. Eshghi, An ultra-low-power 9T SRAM cell based on threshold voltage techniques. Circuits Syst. Signal Process. 35(5), 1437–1455 (2016)
17. S. Naghizadeh, M. Gholami, Two novel ultra-low-power SRAM cells with separate read and write path. Circuits Syst. Signal Process. 38(1), 287–303 (2019)
18. M. Nobakht, R. Niaraki, A new 7T SRAM cell in sub-threshold region with a high performance and small area with bit interleaving capability. IET Circuits Devices Syst. 13(6), 873–878 (2019)
19. H. Okuhara, A.B. Ahmed, H. Amano, Digitally assisted on-chip body bias tuning scheme for ultralow-power VLSI systems. IEEE Trans. Circuits Syst. I Regul. Pap. 65(10), 3241–3254 (2018)
20. S. Pal, A. Islam, Variation tolerant differential 8T SRAM cell for ultralow power applications. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 35(4), 549–558 (2015)
21. G. Pasandi, S.M. Fakhraie, An 8T low-voltage and low-leakage half-selection disturb-free SRAM using bulk-CMOS and FinFETs. IEEE Trans. Electron Devices 61(7), 2357–2363 (2014)
22. M. Sharifkhani, M. Sachdev, Segmental virtual ground architecture for low power embedded SRAM. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 15(2), 196–205 (2007)
23. G. Torrens, B. Alorda, C. Carmona, D. Malagon-Perianez, J. Segura, S.A. Bota, A 65-nm reliable 6T CMOS SRAM cell with minimum size transistors. IEEE Trans. Emerg. Top. Comput. 7(3), 447–465 (2017)
24. B. Wang, T.Q. Nguyen, A.T. Do, J. Zhou, M. Je, T.T.H. Kim, Design of an ultra-low voltage 9T SRAM with equalized bitline leakage and CAM-assisted energy efficiency improvement. IEEE Trans. Circuits Syst. I Regul. Pap. 62(2), 441–448 (2014)
25. Y.Wu, A. Isidori, R. Lu, H.K. Khalil, Performance recovery of dynamic feedback-linearization methods for multivariable nonlinear systems. IEEE Trans. Autom. Control 65(4), 1365–1380 (2019)
26. Y. Ye, M. Khellah, D. Somasekhar, A. Farhang, V. De, A 6-GHz 16-kB L1 cache in a 100-nm dualV/sub T/technology using a bitline leakage reduction (BLR) technique. IEEE J. Solid-State Circuits 38(5), 839–842 (2003)