IMPLEMENTATION OF A 16-BIT APPROXIMATE MULTIPLIER USING APPROXIMATE 5:2 COMPRESSORS

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ABSTRACT

In many applications, multipliers are the one of the most important arithmetic functional units and those applications call for numerous multiplications which consume a lot of power. Employing an approximate multiplier is a growing technique to decrease critical path time and power consumption . In order to decrease the power consumption and delay a multiplier is designed by using the approximate compressors where approximate compressor is used for the data compression. This project explores and proposes the design and analysis of two approximate compressors with reduced area, delay and power with comparable accuracy when compared with the existing architectures. The proposed designs have been extensively verified and projected on scales of power and delay. The proposed approximate 5 : 2 compressor reduced in power, and reduction in delay compared to approximate multiplier using 4 : 2 compressor. The proposed compressors are utilized to 16 × 16 Approximate multipliers The analysis is further extended to project the application of the proposed design in error resilient applications like image smoothing and multiplication.

Keywords: Approximate 4:2 Compressor, Approximate 5:2 Compressor, Approximate multiplier

INTRODUCTION

In VLSI a multiplier refers to a digital circuit that performs multiplication operations on binary numbers. It's a fundamental component used extensively in various computational tasks within digital systems, such as arithmetic operations, signal processing, and data manipulation. The primary function of a multiplier is to take two binary numbers as inputs and produce their product as the output. This operation involves binary multiplication, which is similar to decimal multiplication but simplified due to the limited digit set of 0 and 1 in binary. Multipliers can be implemented using different architectures, each with its advantages in terms of speed, area efficiency, and power consumption. There are many types multipliers like array multiplier, Wallace tree multiplier, Serial multiplier etc. In this paper an approximate multiplier is designed by using compressors like 4-2 and 5-2 where four by two compressor take inputs as four and produce output as two. Similarly five by two compressor take input as five and produce output as two. By using these compressors an approximate multiplier is designed where approximate multiplier sacrifices accuracy for speed, power efficiency, or reduced hardware complexity. It produces an approximate result that is close enough to the exact result for many applications. This paper deals with implementation of a 8-bit approximate multiplier using approximate 4:2 compressor which is existed and along with that we have proposed a 16-bit approximate multiplier which is implemented by using approximate 5:2 approximate compressors. Where compressors are used for the compression of partial products.

LITERATURE SURVEY

Approximate multipliers offer a trade-off between computational accuracy and resource efficiency, making them suitable for applications where minor errors are acceptable. They utilize techniques such as voltage

scaling, reduced precision arithmetic, and error-tolerant algorithms to achieve significant reductions in power consumption and hardware complexity compared to exact multipliers.

A.Momeni, J.han they presents a compelling solution with reduced hardware complexity and lower power consumption compared to traditional multipliers. Further optimizations can enhance its performance for larger operand sizes, making it an attractive choice for high-speed multiplication in various applications. P. Montuschi, and F. Lombardi are proposed the wallace tree multiplier presents a scalable and efficient approach to high-speed multiplication, leveraging parallel processing for reduced latency. Its structured design and optimized partial product reduction make it a preferred choice for demanding computational tasks. Z. Yang, J. Han, and F. Lombardi they presents the 4:2 compressor multiplier offers a balance between accuracy and efficiency, reducing power and area while maintaining acceptable error levels. Its use of compression techniques makes it a viable option for applications prioritizing resource optimization without sacrificing computational performance.

EXISTING METHOD

The above is the diagram of existed 16-bit approximate multiplier using 4:2 compressor where these compressors are having inputs as four and output as two. The constituent blocks of the approximate multiplier, such as the half adders, full adders, and compressors, must first be implemented independently in order to create the 16-bit approximate multiplier. Once the simulation of adders and compressors is finished, a porting operation is required to create an approximate multiplier. Afterwards, waveforms from the designed 16-bit approximate multiplier must be inspected and simulated. Thus, power and delay—two parameters of the multiplier that already exists must be noted.

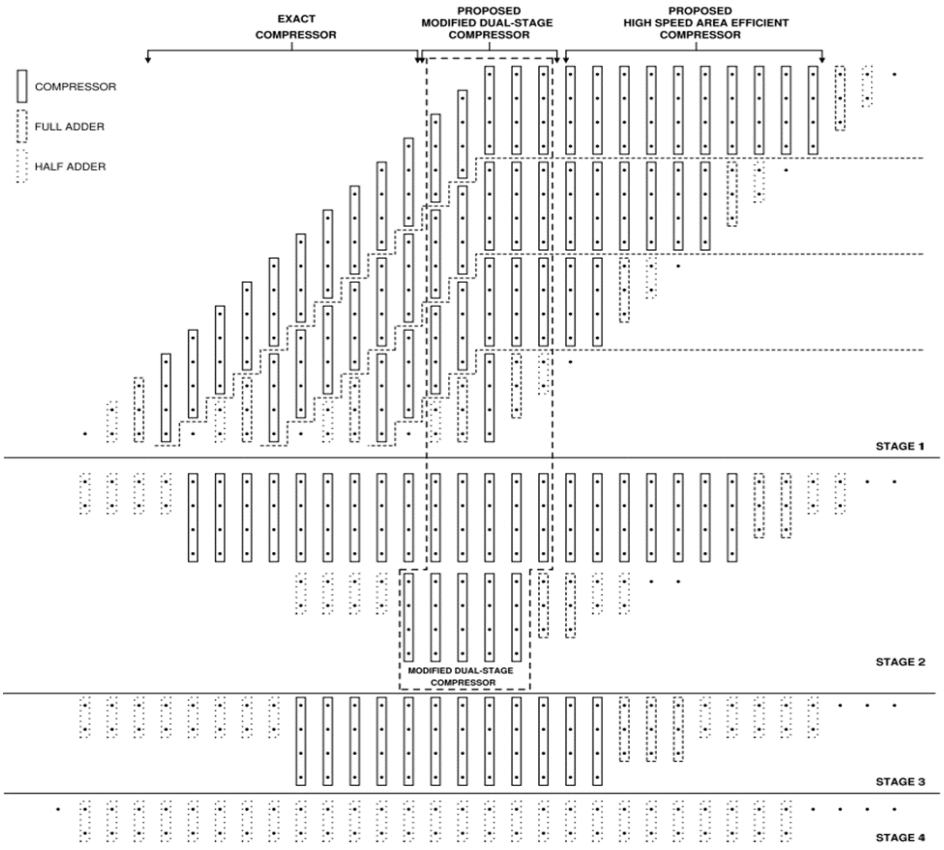

Figure.1 16-Bit Approximate Multiplier using Approximate 4:2 Compressor

PROPOSED METHOD

Initially, a 5:2 approximation compressor is created with logic gates, a mux, and These roughly 5:2 compressors convert five inputs into two outputs. These are specifically employed to compress partial products, which will aid in lowering the specified multiplier's delay and power usage. These area-efficient approximate 5:2 compressors and adders are used to create a 16-bit approximate multiplier following the design of the approximate compressor. This 16-bit approximate multiplier can be implemented in four steps.

The first step generates 16 lines of partial products, each of which is composed of five bits. One compressor is used by the set of five bits, and further partial products are also done and all these compressors generate output as two in stage one. stage one's output is reflected in stage two similarly for the remaining stages it would explained in design structure of multipliers.

The half adders and full adders that make up this suggested multiplier must be implemented independently before the multiplier can be constructed by porting these individual blocks. Compared to the existing 8 bit approximate multiplier, this one requires 16 bits as input, thus it may provide output for larger numbers. This is one of its positive aspects. The suggested multiplier employs an approximate 5:2 compressor, which is more efficient than an approximate 4:2 compressor as it takes five inputs and outputs two. Below figure is the proposed 16 bit approximate multiplier.

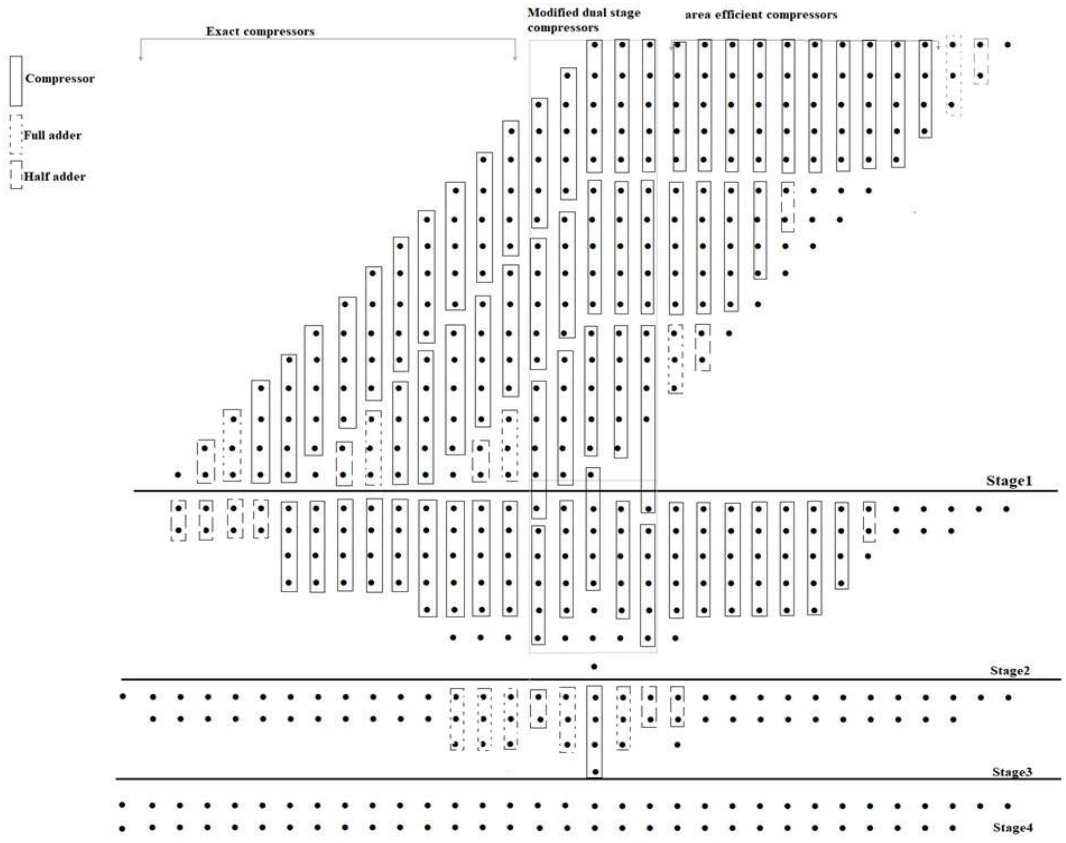

Figure.2.Proposed 16-Bit Approximate Multiplier using Approximate 5:2 Compressors

THE DESIGN STRUCTURE OF THE 16-BIT APPROXIMATE MULTIPLIER

The 16-bit approximate multiplier can be implemented in four steps. The first step generates 16 lines of partial products, each of which is composed of five bits. One compressor is used by the set of five bits, and further partial products are also done and all these compressors generate output as two in stage one. stage one's output is reflected in stage two.

In a manner identical to stage one, stage two groups the partial products, reduces the bits using adders and compressors, and produces output as sum and carry. Similar to how stages one and two group the partial products, adders, and compressors are used to lower the bits and produce output as sum and carry. In a similar manner, stage three reflects the output of stage two.

Lastly, half adders are employed in stage four to generate output as sum and carry. This 16-bit approximation multiplier accepts two inputs, A and B, each of which has a maximum of 16 bits. The multiplier's output is a 32-bit mixture of these two inputs.

RESULT ANALYSIS

The schematic design of the multipliers discussed above are simulated in Xilinx Vivado using 2016.4 as the version. Analyzing the performance of a 16-bit approximate multiplier that uses 5:2 compressors involves evaluating several key metrics related to accuracy, speed, power consumption, and area efficiency specially in real-time systems or those requiring high throughput. Designed 16-bit Approximate Multiplier produce effective delay due to the usage of area efficient approximate 5 to 2 compressors. The speed of the multiplier is crucial in many applications, especially in real-time systems or those requiring high throughput this designed multiplier satisfy the efficiency. Power consumption is a critical concern in modern integrated circuits, particularly for portable devices and energy-efficient systems, power utilized by the designed 16-bit multiplier is low.

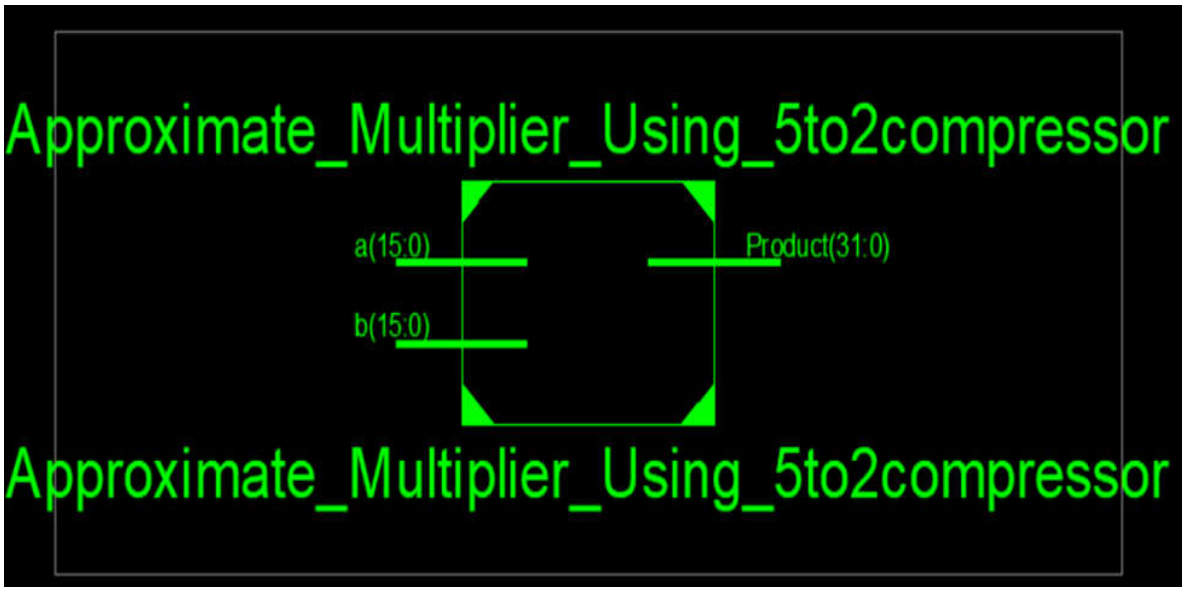

Fig.3. RTL Schematic of 16-Bit Approximate Multiplier

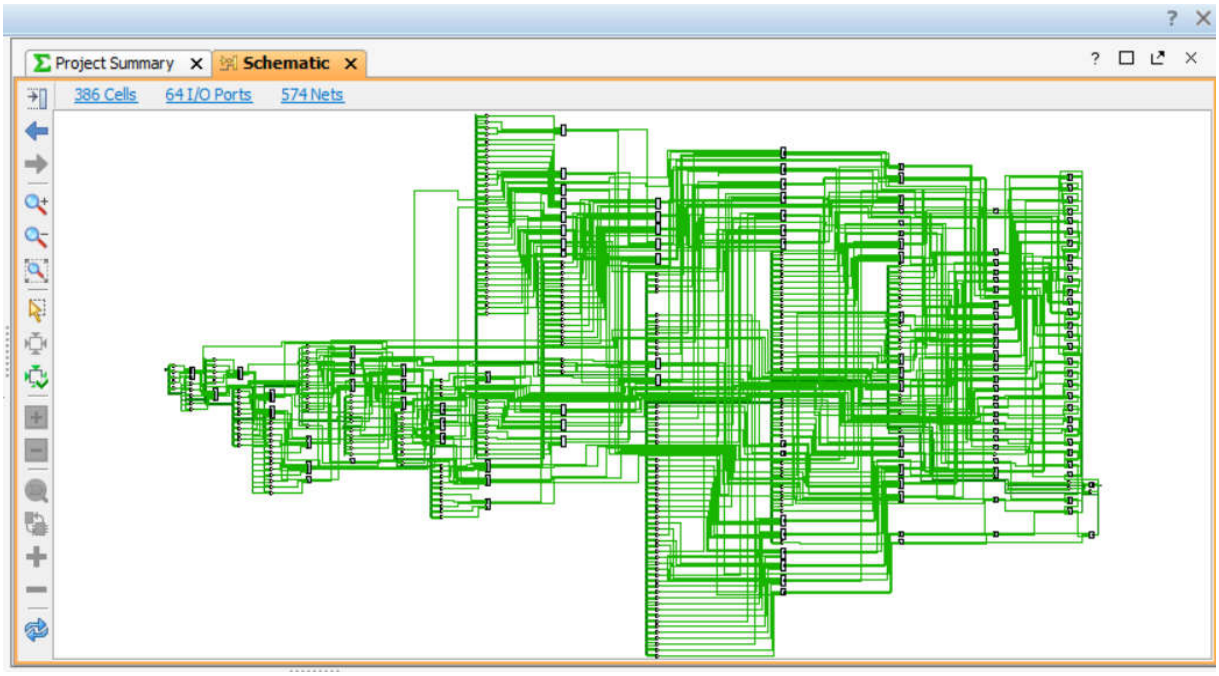

Figure.4. Technology Schematic of 16-Bit Approximate Multiplier

Figure.5. Simulation Result 16-Bit of Approximate Multiplier

Comparison of 16 bit Approximate Multiplier using 4:2 and 5:2 Compressors

PARAMETERS	16-bit Approximate Multiplier using 4:2 compressors	16-bit Approximate Multiplier using 5:2 Compressors
No. of LUT's	298	290
Delay	35.36	32.37
Power(watts)	33.56	30.78

CONCLUSION

The design and study outcomes of the approximate multipliers for machine learning and image processing applications are discussed in this paper. By writing the code in Verilog Hdl, the 16-bit approximation multiplier's simulation results can be seen in the Xilinx Vivado software. In addition to the amount of lookup tables and latency, the power results of the 16-bit approximate multipliers are noted. In comparison to the 16-bit approximate multiplier using 4:2 compressors, the 16-bit approximate multiplier utilizing 5:2 compressors has a higher compression ratio.

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