RADIATION-HARDENED LOW-POWER SRAM: A DUAL-NODE UPSET RESILIENT SOLUTION FOR AEROSPACE APPLICATIONS

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ABSTRACT

This project presents the design and implementation of an energy-efficient dual-node upset recoverable 127-bit Static Random-Access Memory (SRAM) for low-power aerospaceapplications. The proposed SRAM architecture combines dual-node technology to enhanceradiation tolerance and upset recovery mechanisms to mitigate the impact of single-eventupsets (SEUs) caused by cosmic rays or high-energy particles. This reduction make SRAMcells used for aerospace applications more susceptible to radiation as it can cause single event upsets (SEUs) and also single-event multi-node upsets (SEMNUs).This work presents a robust and highlyreliable 1.2 V 10-Transistor (10T) Static Random Access Memory (SRAM) cell designed witha focus on Radiation Hardened by Design (RHBD) principles for aerospace applications. Thedemand for electronic components that can withstand harsh radiation environments in spacemissions has necessitated the development of memory cells capable of mitigating single-eventupsets and other radiation-induced faults. 10T SRAM cell leverages RHBD techniques toenhance its resilience to radiation-induced errors. The cell design incorporates redundant pathsand latch structures to minimize the vulnerability of critical nodes, providing a robust solutionfor aerospace applications where reliability is paramount. The design will be simulated at adifferent supply voltages and different performance for metrics like read power, write power,write delay, read delay, leakage power and critical charge will be evaluated. All Designs willbe in implemented in 45nm technology using tanner tool version.

INTRODUCTION

SRAM is one of the many types of computer memories that is used extensively in both analog and digital electrical systems[1].Satellites ever-increasing need for complicated functionality needs increasingly complex components and lighter packaging containing larger capacity memories.Lightweight satellites need high density memory cells due to their limited size. Because of its high packing density and enhanced logic performance in digital data processing and the satellite control system, SRAM cells are an ideal choice for this kind of application. Applications that demand faster speeds and lower power usage employ SRAM. Nearly every SRAM component is created using CMOS technology.When high energy particlessuch as protons, neutrons, alpha particles, or other heavy ion particlesthat are prevalent in high-altitude, natural space, or terrestrial environments impact a sensitive node within an integrated circuit (IC), it might result in a single event effect (SEE).In environments with high radiation levels, such as space and military applications, soft error brought on by radiations make it difficult for an electronic system to function reliably.The higher sensitivity volume per bit and lower node capacitance in static random-access memory (SRAMs), the likelihood of these single event upsets (SEUs) is very high [2]. In sequential circuits, the soft error is an important issue that leads to bit flipping in memory elements (latches, flipflops, SRAM, etc.).In other words, values recorded in SRAMs may be erroneously changed by soft

mistakes.As a result, over the last four decades, numerous authors have been dedicated to reducing these soft errors by introducing system-level, layout-level, and circuit-level mitigation approaches. Among the three levels of mitigation approaches, circuit-level mitigation is simple, reliable, and achieves a greater critical charge approach [3].Even though constructing a circuit for an extensively radiative atmosphere, there is a trade-off with reliability (critical-charge) between power-dissipation, speed, and manufacturing cost. Circuit-level SRAM design has not only provided higher fault tolerate abilities (robustness) but also lower expenses when compared to layout- and system-level hardening methodsin order to get the best overall cost while making radiation-hardened SRAM, other performance characteristics must be maintained within a reasonable range.At the circuit level, the SRAM bit-cell is changed to incorporate extra devices in order to minimize the data interruptions brought on by SEU [4].

EXISTING SRAM CELLS

6T SRAM Cell:

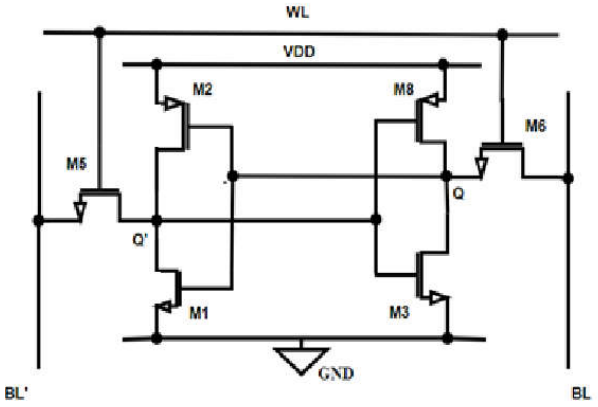

Fig 1: 6T SRAM CELL

The 6T SRAM CELL consists of a back to back CMOS inverters,CMOS inverter acts as a NOT gate i.e., the output is the complementary of the given input. Hence when the input is given as logic"1" the output will be logic"0" and vice versa.It consists of a Sense amplifier which compares the difference between BL and BLB,If BL>>BLB then output will be "1", i.e., BLB>>BL then output will be "0".

READ OPERATION:

When the word line is given as "1" then the access transistors M3 and M4 are switched ON. The access transistors act as a short circuit. In read operation we have two cases. When QB=1 and Q=0,Then QB=1 and WL=1,hence there is no voltage difference at BLB, at the same time Q=0 and WL=1,hence there is a voltage difference at BL.Therefore BLB >>BL,the output will be "0" When QB=0 and Q=1.

Then QB=0 and WL=1,hence there is no voltage difference at BLB, at the same time Q=1 and WL=1,hence there is a voltage difference at BL.Therefore BL>>BLB,the output will be "1".

WRITE OPERATION:

When the word line is given as "1" then the access transistors M3 and M4 are switched ON.The access transistors act as a short circuit.In Write operation we have two cases. Here

the inputs will be BL and BLB,When BL=0 and BLB=1,then Q=0 and QB=1,When BL=1 and BLB=0,then Q=1 and QB=0.

HOLD OPERATION:

During hold operation WL=0 then BL and BLB are discharged from the latch circuit.

10T SRAM CELL:

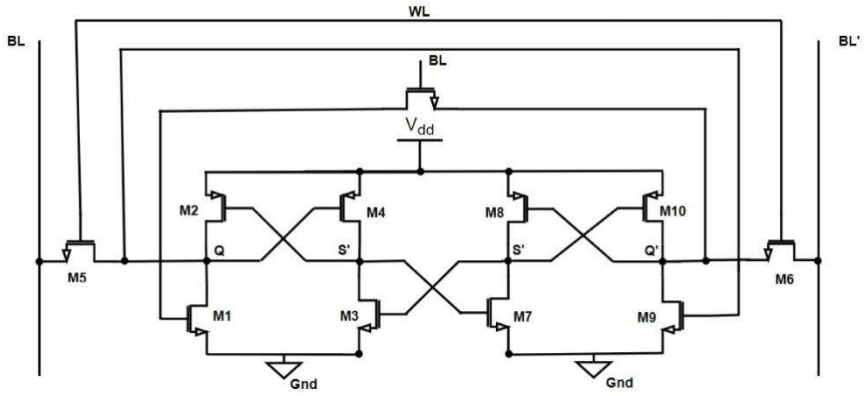

Fig 2: 10T SRAM CELL

Static random-access memory (SRAM) cells with ten transistors are called 10T SRAM cells. Compared to conventional 6T SRAM cells, it provides benefits including increased stability and low leakage, which allows it for low-power applications in contemporary integrated circuits.

READ OPERATION:

The cell consists of four PMOS and four NMOS and two access transistors. The transistors are controlled by row-based WL signal and used for read and write operation.During the read operation both the bit lines (BL and BLB) are charged to Vdd through the prechargedcircuitry.The word line that is attached to the SRAM cell is engaged when a read operation is commenced. The storage node can now be connected to the bit lines (BL and BLB) as a result of the activation of the access transistors. Thebit line attached to the storage node will be discharged if it has a high voltage (corresponding to a logical "1"), but the complimentary bit line will stay charged. On the other hand, the opposite will happen if the storage node has a low voltage (signalling a logical "0"). The corresponding bit line will discharge while the bit line is still charged. After detecting the voltage difference between the bit lines, sense amplifiers enhance the signal to reveal the data that has been stored. For the accomplishment of successful read operation, the access transistor must be kept weaker than the pull-down transistor.

WRITE OPERATION:

During a write operation, the data to be written is first driven on to the bit lines (BL and BLB). Next, the word line attached to the SRAM cell is turned ON. Now consider the write 1 operation as per the assumption made in the read operation. Thebit lines data can be stored in the storage node because the access transistors are activated. Based on the data on the bit lines of BL being high and BLB being low, the voltage of the storage node is changed to a high voltage (logical "1") and vice versa. Mechanisms for precharging make sure that the bit-lines

are at the proper voltages prior to writing Preventive measures, Interference with current data. Toachieve a successful, write operation, the access transistor should be kept stronger than the pull-up transistor.

HOLD OPERATION:

The 10T SRAM cell maintains the stored data by holding its state in between read and write operations. The storage node and the access transistors have feedback loops that ensure the retention of stored data. By acting as isolation mechanisms, the access transistors stop unwanted leakage routes that can destroy the data that has been stored. Since the cell is not actively reading or writing data, power is used very little when the hold action is in operation.

12T SRAM CELL:

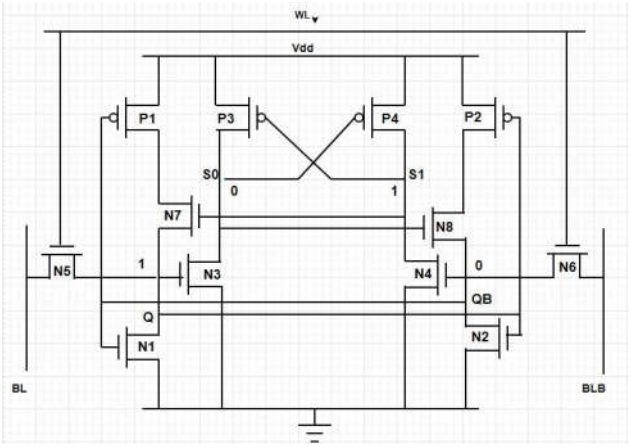

Fig 3: 12T SRAM CELL

A Static Random Access Memory (SRAM) cell with 12 transistors for access and storing is known as a 12 T SRAM cell. These cells are commonly found in high-performance components like CPUs and cache memory, where dependability and speed are essential. Because they have more transistors than conventional 6T SRAM cells, they are more stable and less susceptible to disturbances, which makes them appropriate for high-end computing applications.

READ OPERATION:

When a read operation is initiated, the word line connected to the SRAM cell is activated.Bit lines are initially precharged to Vdd during read mode and WL is clamped at Vdd.The access transistors are turned ON, which allows the storing node to be connected to the bit lines (BL and BLB). It detects the voltage difference between the bilinitebit line that is connected to a storage node which is holding a high voltage discharge while the complimentary bit line stays charged. On the other hand, the opposite happens if the storage node has a low voltage. When a 50mv potential difference is attained between the bit lines stored data is sensed.Sense amplifiers, identify and amplify the variation in voltage between the bit lines, precisely identifying the data that has been stored.

WRITE OPERATION:

The bit lines (BL and BLB) are first used to drive the data that will be written. Next, the word line that is attached to the SRAM cell is turned on. The bit lines data can be placed in the storage node as the access transistors are now operational. The voltage at the storage node

is changed in accordance with the voltages that are present on the bit lines. For instance, the storage node is set to a high voltage (Logical1') if BL is high and BLB is low, and vice versa. In order to avoid interfering with already-existing data, precharging systems make sure that the bit lines are at a certain voltage before the write operation.

HOLD OPERATION:

Both the access transistors are biased to be in the cut-off region, and the bit lines are precharged to Vdd during hold mode to reduce the wake-up delay. A 12T SRAM cell that is in hold mode preserves its stored data without updating or changing it. The information contained in the cell must be kept there when the memory is not being actively read or altered, which requires this action. Together, the cells 12 transistors maintain the stability of the stored state and guard against data loss. The hold operation makes sure that the data in the memory doesn't get read or changed until a later access action.

Quatro10T SRAM CELL:

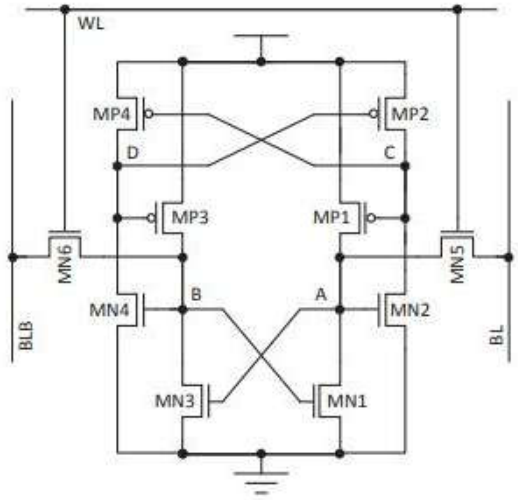

Fig 4: Quatro 10T SRAM CELL

Quatro 10T SRAM cell is a combination of 6 NMOS and 4 PMOS Transistors. Formed by Two inverters by cross-coupling pairs of NMOS and PMOS Transistors.

READ OPERATION:

When the word line is activated the access transistors N5 and N6 are turned ON. When bit line BL=1 logical'1' is passed through transistor P1 it gives logical '0' then it is passed through the MP2 transistor it gives the output at node D as logical '1' at the same time when bit line BLB=0 logical'0' is passed through transistor N6 which gives a logical'0', then it is passed through the transistor P3 which gives a logical'1', then it is passed through the transistor P4 transistor which gives the output at node C as logical'0'. Hence when BL-1 and BLB=0 then C=0 and D=1 at the same time when BL=0 and BLB=1 then C=1 and D=0.Quatro 10 T cell consumes 26% Less leakage current.

WRITE OPERATION:

In write operation, the proposed NMOS stacked 10T SRAM cell is driven to the new logical value by both bit lines (BL and BLB) For writing 0, BL and BLB are precharged to '0' and '1' respectively, and the WL is activated. Once WL is high.BL pulls down the potential at node B.Because the response of P1 and P3 transistors depends on the nodes A and B.MN1 and MN3 are turned OFF directly by the current driven by P1 andP3 respectively.

HOLD OPERATION:

A Quatro 10T SRAM cell retains its stored data while it is in hold mode; it is not refreshed or altered. The state of the cell is retained, along with the extra stable states that exist outside of the conventional binary 0 or 1. By performing this procedure, it is ensured that the data is preserved even in the absence of active access or manipulation to the memory. In applications where power consumption needs to be kept to a minimum, like in mobile or Internet of Things devices, the hold operation's stability is crucial for dependable data retention and integrity.

RESULT AND ANALYSIS:

OPERATION	SRAM	0.8V	0.9V	1V
WRITE '1' DELAY(nS)	6T	0.57	0.52	0.4
	10T	0.58	0.53	0.53
	12T	0.7	1.1	5.3
	QUATRO10T	0.8	0.8	0.7
WRITE '0' DELAY(nS)	6T	0.55	0.50	0.7
	10T	10.4	10.5	10.4
	12T	10.4	10.4	10.3
	QUATRO10T	0.1	0.9	19.8

Fig.(a) Delay (in nS)

OPERATION	SRAM	0.8V	0.9V	1V
WRITE '1' POWER(nW)	6T	0.001	0.002	0.0028
	10T	0.007	0.0054	0.0034
	12T	0.002	0.005	0.009
	QUATRO10T	422.6	480.3	483
WRITE '0' POWER(nW)	6T	0.52	0.76	0.001
	10T	988.9	0.0014	0.001
	12T	0.005	0.012	0.02
	QUATRO10T	418.6	431.4	444.3

Fig.(b) Power Consumption (in nS)

OPERATION	SRAM	0.8V	0.9V	1V
READ DELAY(nS)	6T	5.4	3.2	2.2
	10T	2.08	1.3	1.01
	12T	5.5	3.2	2.2
	QUATRO-10T	5.6	3.3	2.4
READ POWER(nW)	6T	1.42	2.2	2.03
	10T	19.4	35.8	28.1
	12T	10.3	19.1	24.1
	QUATRO-10T	19.07	37.5	25.3

Fig.(c) Read Delay & PowerFig.(d)POWER DELAY PRODUCT (in fm) (write"1")

SRAM Cells	0.8v	0.9v	1v
6T	0.0029	0.006	0.8
10T	0.4	0.7	0.9
12T	57.8	125.3	220.6
Quatro 10T	0.08	0.4	8.7

SRAM Cells	0.8v	0.9v	1v
6T	29	26.6	30.9
10T	0.0012	0.00122	0.0013
12T	15.3	17.2	20.1
Quatro 10T	520	492	478

Fig.(e) CRITICAL TIME (in nP)

CONCLUSION

The simulation of 6T,10T, 12T, Quatro-10T SRAM cells has been carried out successfully with the help of Tanner tools in 45nm technology.The compared parameters were read delay, write delay(write'1', write'0'), power consumption and Critical time.The 6T SRAM cell consums low power ,Delay and Critical Time less compared to 10T,12T and QUATRO 10T SRAM Cell.

Reduction in the power consumption reduces the problems associated with high temperature and also provides an additional benefit in terms of the extended life of the battery.

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