

“DESIGN AND VALIDATION OF SKY-TCAM: LOW POWER SKYRMION BASED TERNARY CONTENT ADDRESSABLE MEMORY”

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ABSTRACT

Skyrmions are mostly utilized for magnetic materials and data storage. Magnetic skyrmions are topologically stable nanoscale spin structures that could be used to construct future spintronic devices. Skyrmion has unique qualities such as nanomaterial diameter and current controlled motion. Skyrmion's unusual features make it an attractive candidate for innovative memory applications that carry information bits of both 0 and 1. Skyrmion-based ternary CAM (Sky-TCAM) cell that is fast, compact, and requires little power. Each cell's 5T2R structure consists of two magnetic tunnel junctions (MTJ) and five transistors. The XOR logic can be accomplished by utilizing the search current polarity and the stored bit. When a mismatch occurs, the matchline (ML) is released, and the skyrmion appears beneath one MTJ.

INTRODUCTION

Content addressable memory (CAM) is different from conventional memory as we feed the data to be searched and the memory returns the address where the searched content is present unlike other memories where the address to be searched is fed and the data in that address location is retrieved. Ternary content addressable memory (TCAM) is an added functionality to CAM which support the functionality to store and search don't care term $_X$ apart from $_1$ and $_0$. The advantage of TCAM is that the entire search operation happens in a single cycle instead of multiple clock cycles in other memories such as SRAM. Hence TCAM finds wide variety of uses such as in look up tables, network routers, wearable devices, and other operations which require searching large data at high speed. A TCAM cell consists of a cross coupled inverter structure similar to SRAM, and the search operation is fast and reliable. However its drawback is static power consumption due to the parallel search structure, which increases the overall power factor of TCAM. This is a major issue for it to be used in battery operated and power critical applications.

EXISTING SYSTEM

The NOR cell that has been presented is TCAM cell. This cell can store either logic $_0$ or logic $_1$. In addition, it can store an $_X$ value. The $_X$ value is a don't care, that represents both $_0$ and $_1$, allowing a wildcard operation. When a cell contains a value of "X," it operates as a wildcard, meaning that any bit in the input will result in a match. Figure 1 shows a NOR-type TCAM cell. The bit storage in both cases is two SRAM cells where cross-coupled inverters implement the bit-storage nodes A and B. Typically, CAM cells use SRAM storage which is volatile in nature. The NOR and SRAM implement the bit comparison, which is conceptually similar to an XOR of the stored bit and the search bit, slightly differently and the NAND cells. It is possible to encode a ternary symbol into two bits. We represent these two bits as A and B. Note that although the A and B are not necessarily complementary, we maintain the complementary notation for consistency with the binary CAM cell. We exclude the state in which A and B are both zero because two bits can represent four possible states, whereas ternary storage only needs three states. To store a ternary value in a NOR cell, we need two SRAM cells. One bit, A, connects to the left pull down path and the other bit B, connects to the right pull down path, making the pull down paths independently controlled. We store an $_X$ by setting both A and B equal to logic $_1$, which disables both pull down paths and forces the cell to match regardless in the inputs. We store a logic $_1$ by setting A=1, B=0 and store a logic $_0$ by setting A=0, B=1 and In addition to storing an $_X$, the cell allows searching for a "X" by putting logic "0" and SL in place. This is an external don't care that forces a match of a bit regardless of the stored bit.

The left end of nanotrack is connected to the transistor T_5 that controls the writing current from WR and WR through WL. The nanotrack resistances are R_n ($n=1-5$). The two MTJs (R_{MTJ1} , R_{MTJ2}) on top of the nanotrack are connected to ML through T_1-T_4 transistors. T_1 , T_2 form the controlled discharge paths for ML, and the drains of T_3 and T_4 are connected to the search lines (SL, SL) where the input query is provided. Write Operation: Data is written into the TCAM by setting the magnetic state of each MTJ in the memory cells according to the desired data values. This typically involves applying appropriate magnetic fields or currents to switch the polarity of the magnetic domains within the MTJ for each cell. Read Operation: During a read operation, the resistance state of each memory cell is sensed by passing a read current through the MTJ and measuring the resulting voltage. The resistance state corresponds to the stored data value, allowing for data retrieval. Comparison Operation: When performing a search operation, the stored data in each memory cell is compared in parallel with the corresponding bits of the search key. This comparison determines if there's a match between the stored data and the search key. Based on the comparison results, the TCAM outputs the addresses of the matching cells or any associated data stored along with them, providing information about the location of the matched data within the memory array. Control and Timing: Dedicated control logic manages the timing and sequencing of write, read, and compare operations to ensure proper functionality and coordination within the TCAM.

RESULTS

Simulations would likely investigate how skyrmions form within the memory cells and assess their stability under different temperatures, magnetic fields, and material properties. Understanding the conditions under which skyrmions form and remain stable is crucial for reliable memory operation.

Write and Erase Operations: Simulations would explore how data is written into the Skirmion TCAM cells by manipulating the positions or properties of skyrmions. This involves applying localized magnetic fields or currents to induce skyrmion motion and alter the magnetic state of the memory cell. Similarly, simulations would assess the efficiency of erasing data by resetting the magnetic state of the cells.

Readout Mechanism: Skyrmion TCAM relies on detecting the presence or absence of skyrmions to read stored data. Simulations would evaluate the readout process, including how skyrmions are detected and how the stored information is retrieved from the memory array. Noise and Reliability: Simulations would also consider the impact of noise, defects, and environmental fluctuations on the performance and reliability of Skyrmion TCAM. This involves assessing error rates, retention times, and overall robustness of the memory cells under realistic operating conditions. Speed and Energy Efficiency: Another important aspect of simulation results would be the evaluation of the speed and energy efficiency of Skyrmion TCAM compared to existing memory technologies. This includes analyzing access times, power consumption, and scalability to larger memory arrays. One significant advantage of Skyrmion-TCAM is its inherent parallelism, allowing for simultaneous processing of multiple search queries. This parallelism arises from the collective behavior of Skyrmions, which can interact with each other within the magnetic medium. As a result, Skyrmion-TCAM architectures exhibit high throughput and low latency, making them suitable for applications requiring real-time data processing. Furthermore, Skyrmion-based TCAM offers non-volatile operation, enabling data retention even in the absence of power. This feature enhances the resilience and reliability of computing systems, particularly in environments prone to power outages or disruptions. Additionally, Skyrmion-TCAM cells exhibit robustness against external perturbations, such as electromagnetic interference, ensuring reliable operation in diverse operating conditions.

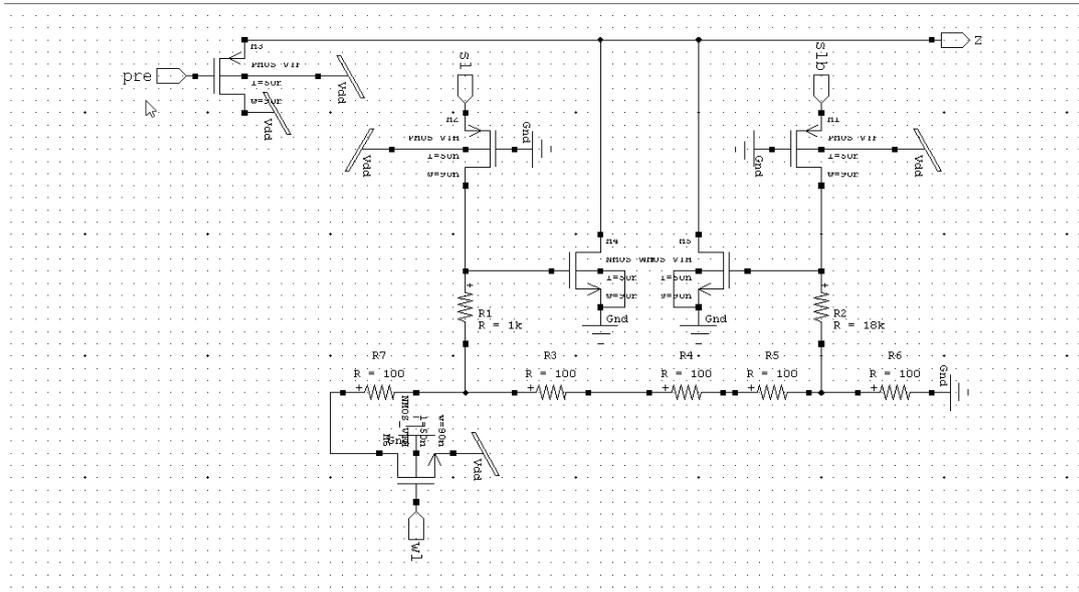


Fig.3 Schematic diagram of SKYRMION-TCAM

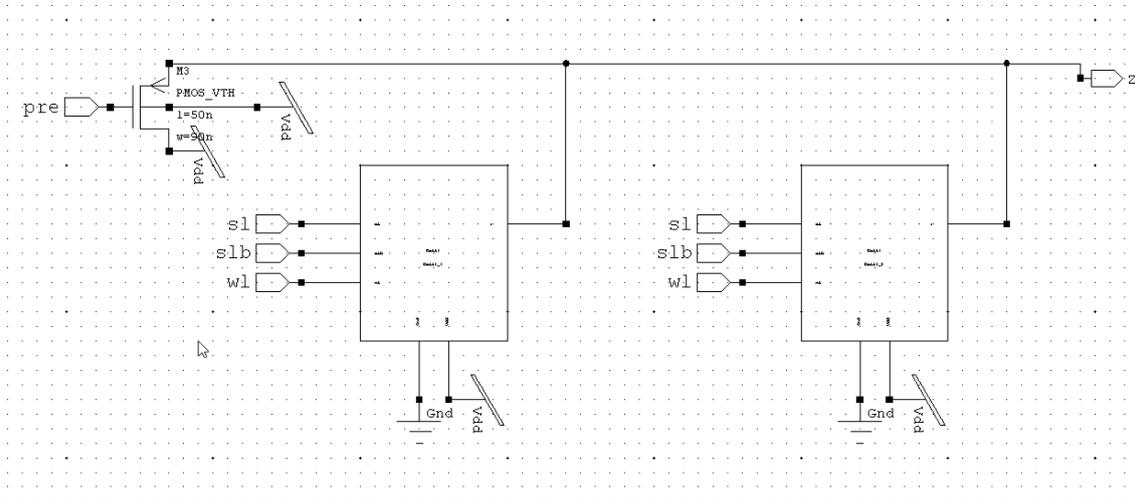


Fig : 4 Circuit of SKY-TCAM 2Cell

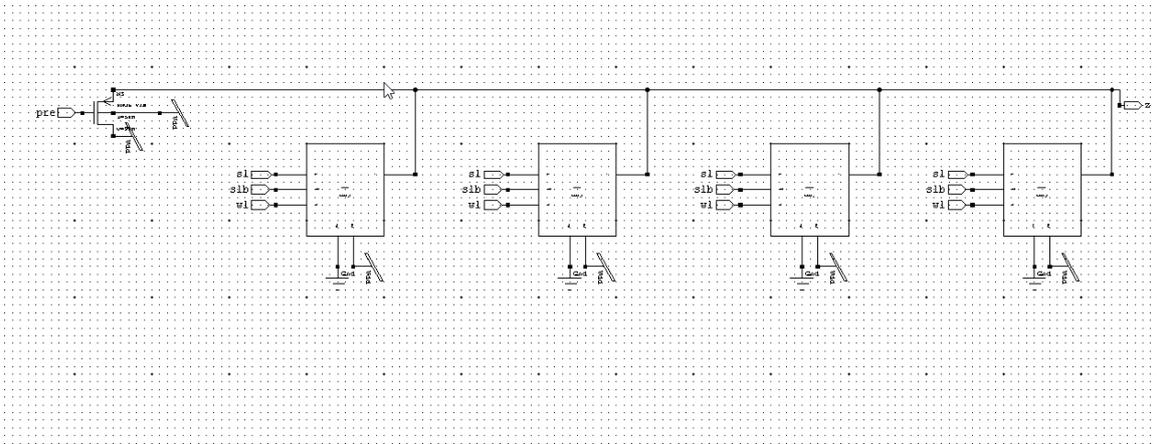


Fig : 5 Circuit of SKY-TCAM 4Cell

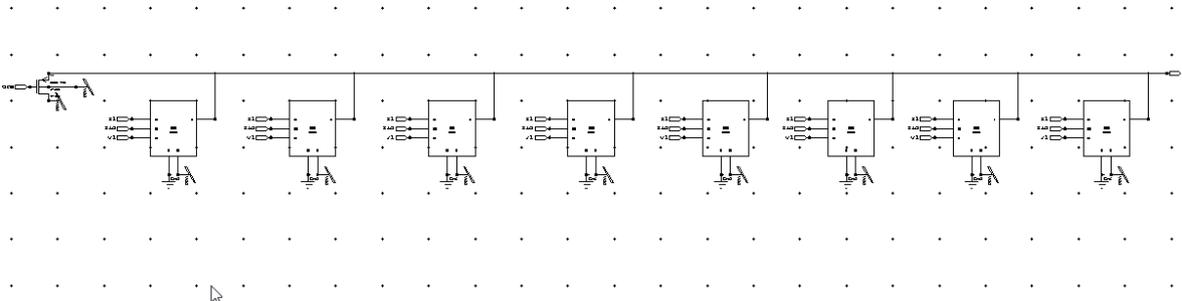


Fig :6 Circuit of SKY-TCAM 8 Cell

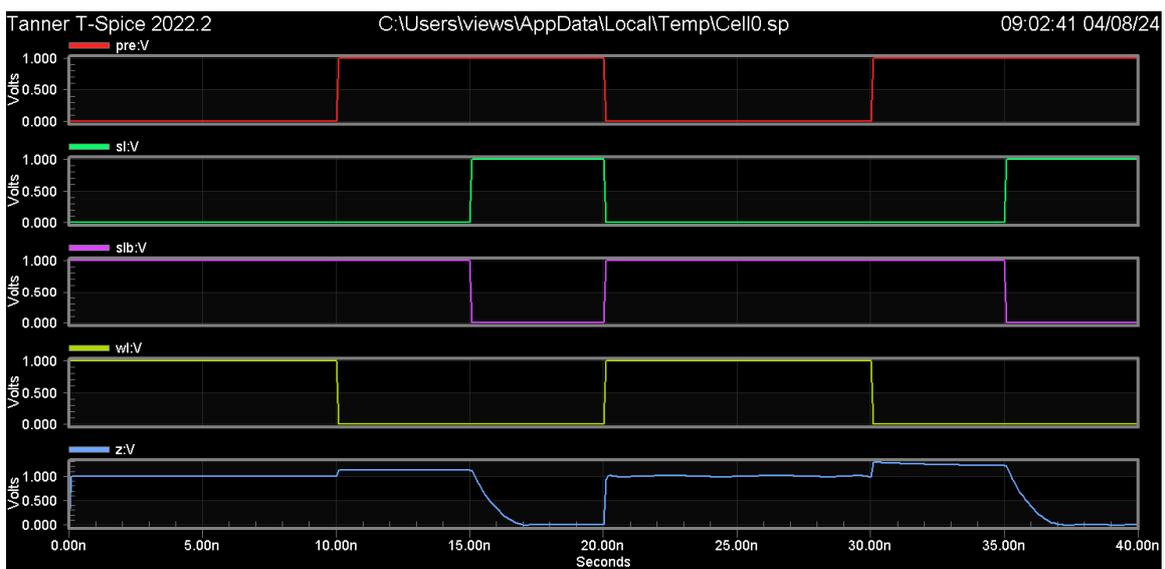


Fig : 7 Schematic results of 0 Stored Skyrmion TCAM

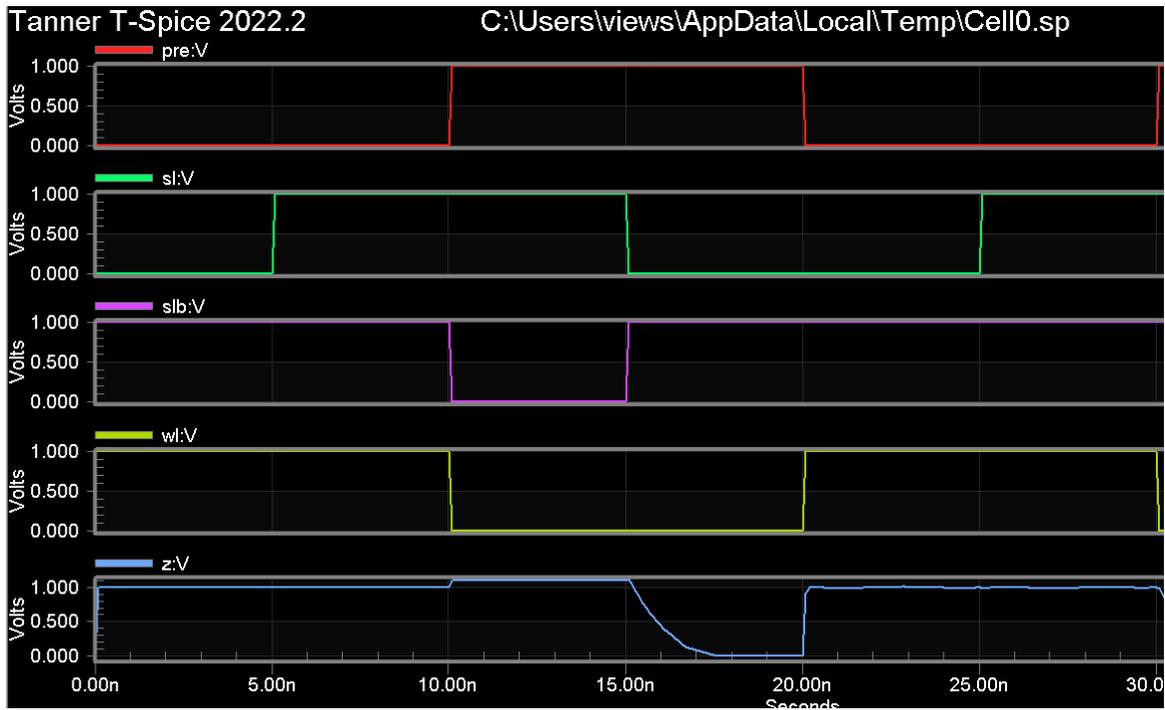


Fig : 8 Schematic results of 1 Stored Skymion TCAM

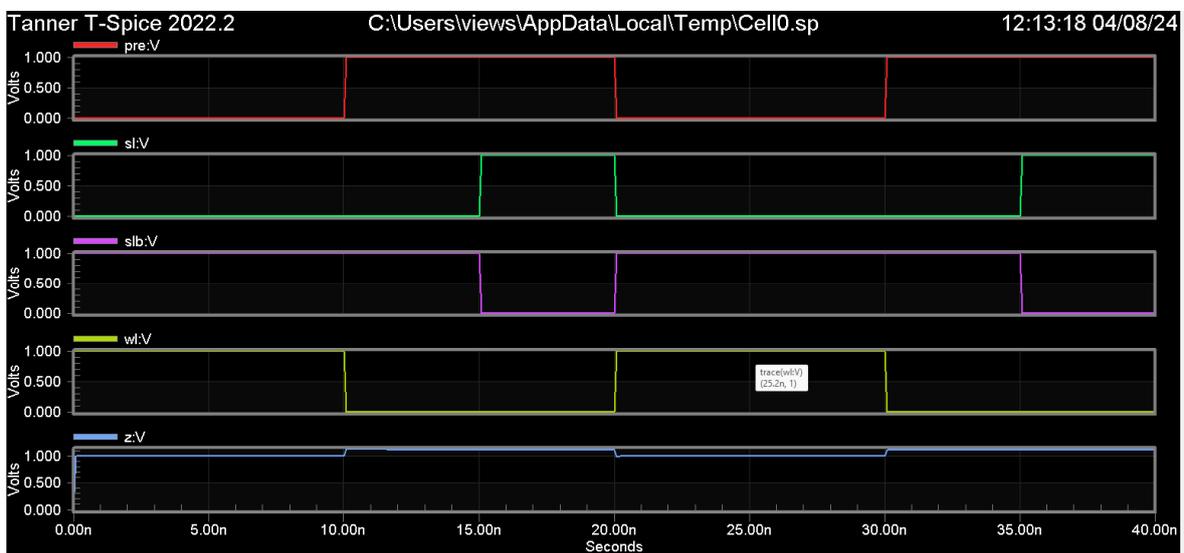


Fig : 9 Schematic results of Don't care Skymion TCAM

COMPARISION BETWEEN NOR-TCAM AND SKYRMIION TCAM

CELLS	NOR TCAM		SKYRMIION TCAM	
	POWER (micro watts)	DELAY (nano sec)	POWER (micro watts)	DELAY (nano sec)
1 CELL	5.3	1.9	4.5	1.4
2 CELL	6.8	1.9	5.20	1.4
4 CELL	8.10	1.93	5.21	1.4
8 CELL	9.09	1.99	6.1	1.4

CONCLUSION

In this paper, the design and analysis results of the comparators have been presented for CMOS flash ADC applications. The simulation results of the various CMOS comparators are obtained incidence virtuoso using 18nm technology and compared with each other for performance evaluation. By contrast, the propagation delay and power dissipation of a TIQ comparator are low. And the use of transistors is also less compared to all other comparators. Low voltage comparator used less transistor count next to TIQ comparator but it takes large power compared to TIQ comparators. Different kinds of comparators use a comparatively high number of transistors counted in the comparison.

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