Design and Implementation of Symmetrical Multi-Level Inverters

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ABSTRACT

Multi-level inverters have become the industry standard and indispensable for many industrial applications in the field of DC/AC inverters. With the advent of sophisticated medium-power self-commutated switching devices, multi-level inverters (MLIs) are becoming more widespread. The main benefits of MLIs include decreased total harmonic distortion (THD), input filter reduction, less stress on switches, decreased dv/dt , lower di/dt, operating at both higher and lower switching frequencies, decreased power losses, increased power process capability, improved overall efficiency, and decreased electromagnetic interference (EMI). The architecture that is being given has a polarity changer, a level generator, and the fewest DC sources. A polarity switcher is an H-bridge. Electrical switches are used in polarity changers and level generators. By adding more cells and switches to a level generator, output levels can be increased even more. This study is focused on minimizing the switch count and voltage sources by implementing symmetrical setups of the multilevel inverter. The multilevel inverter was intended for use with a symmetrical 5-level inverter. To verify the practicality of the proposed system, simulation verification is carried out using experimental findings, and total harmonic distortion (THD) is noted for both MLI configurations. A hardware prototype is developed in the lab, and the constant load condition is empirically confirmed.

KEYWORDS:H-Bridge, Multilevel Inverter, Symmetrical Inverter.

INTRODUCTION

A Symmetrical multi-level inverter is a type of power electronic device used to convert DC (direct current) voltage into AC (alternating current) voltage with multiple levels. Unlike traditional two-level inverters, which switch between two voltage levels (positive and negative), symmetrical multi-level inverters utilize several levels of DC voltage to synthesize a stepped waveform, resulting in reduced harmonic distortion and improved voltage quality. This technology is crucial for high-power applications where maintaining high efficiency and minimizing harmonic content are paramount. Common topologies include diode-clamped, flying capacitor, and cascaded H-bridge configurations, each offering unique advantages in terms of scalability, voltage capability, and complexity. The operation of a symmetrical multi-level inverter involves sophisticated control strategies such as pulse width modulation (PWM) or selective harmonic elimination (SHE), which ensure precise regulation of the AC output waveform. Applications of symmetrical multi-level inverters span a wide range, including renewable energy systems (like solar and wind power), electric vehicle drives, motor control, and grid-connected power systems. The development and optimization of these inverters are driven by the need for efficient, reliable, and environmentally friendly power conversion solutions in modern electrical engineering and industrial applications. Ongoing research focuses on enhancing the performance, reducing the cost, and expanding the scalability of symmetrical multi-level inverters to meet the evolving demands of the power

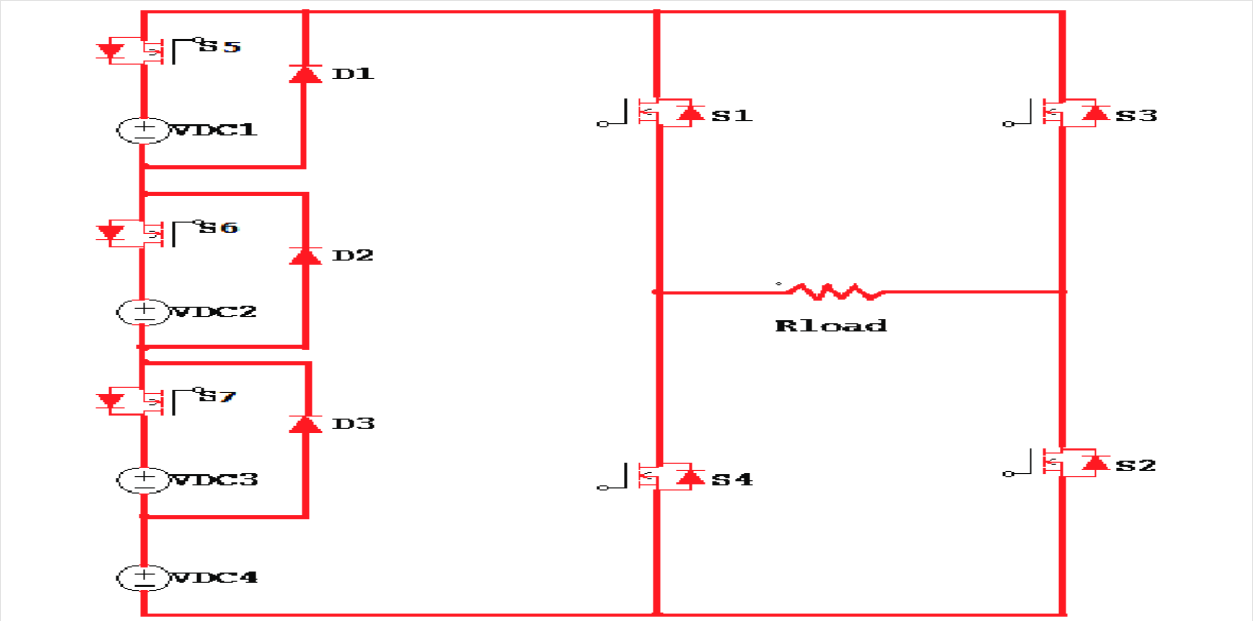
electronics industry.

LITERATURE SURVEY

The literature survey conducted for the symmetrical multi-level inverter project encompassed a comprehensive review of existing research and developments in the field of multi-level inverters. This survey commenced with an introduction outlining various multi-level inverter topologies, including diode-clamped, flying capacitor, and cascaded H-bridge configurations, emphasizing their advantages over conventional two-level inverters such as reduced harmonic distortion and improved voltage capabilities. Subsequently, a detailed analysis of control techniques was undertaken, focusing on modulation strategies like sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE), and space vector modulation (SVM), evaluating their complexity, performance, and practical feasibility. Additionally, the survey explored diverse applications where multi-level inverters demonstrate efficacy, such as renewable energy systems, electric vehicle drives, and high-power motor control, supported by case studies illustrating performance enhancements in these domains. Recent advances and emerging trends in multi-level inverter technology were also investigated, alongside discussions on challenges like increased complexity and cost, with proposed mitigation strategies from the literature highlighted. Comparative evaluations of different topologies based on efficiency, total harmonic distortion (THD), and cost-effectiveness provided valuable insights into their strengths and limitations. The survey concluded by identifying gaps in current research and outlining future directions for optimization of control strategies, integration with smart grid technologies, and enhancement of reliability, contributing to the project's foundation and guiding its objectives towards innovative advancements in symmetrical multi-level inverter design and implementation.

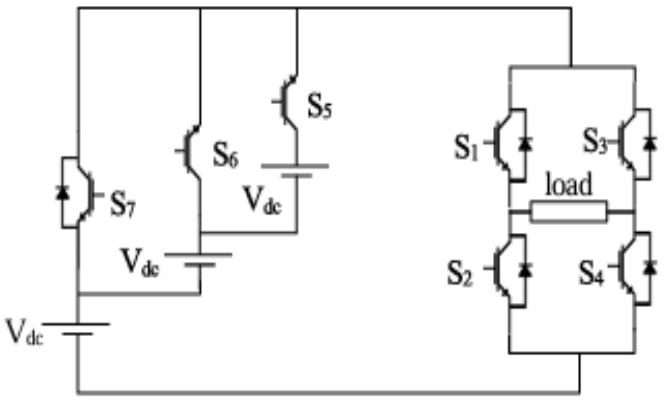
EXISTING METHOD

Existing symmetrical multi-level inverter systems encompass a range of established topologies tailored for different applications and performance requirements in power electronics. Diode-clamped (or neutral-point clamped) inverters utilize diodes and capacitors to create multiple voltage levels, offering simplicity and reliability but with potential drawbacks related to component size and cost. Flying capacitor inverters achieve multi-level output by switching capacitors in various combinations, delivering good performance with reduced switching losses but requiring precise capacitor voltage balancing. Cascaded H-bridge inverters, consisting of multiple H-bridge cells connected in series, provide scalability and modular flexibility in voltage levels and power ratings. Neutral-point clamped (NPC) inverters feature a midpoint in the DC link, reducing voltage stress on components and enabling efficient handling of medium to high-power applications. Ongoing research explores alternative and hybrid configurations to optimize efficiency, reduce costs, enhance reliability, and expand the applicability of symmetrical multi-level inverters, particularly in renewable energy systems, electric vehicles, and industrial drives. The selection of a specific topology depends on factors such as power rating, voltage requirements, switching frequency, and cost-effectiveness, reflecting the diverse landscape of symmetrical multi-level inverter designs in contemporary power electronics.



Symmetrical Multi Level Inverter

PROPOSED SYSTEM



A proposed system for a symmetrical multi-level inverter aims to leverage advanced power electronics technology to efficiently convert DC power to high-quality AC output suitable for various applications such as motor drives, renewable energy systems, and grid-connected devices. The system design incorporates multiple voltage levels generated from a series of power electronic switches arranged in a cascaded configuration.

In this proposed system, the core architecture includes several H-bridge modules, each consisting of pairs of insulated gate bipolar transistors (IGBTs) or metal-oxide-semiconductor field-effect transistors (MOSFETs) with diode clamps. These modules are stacked in series to achieve the desired number of output voltage levels. For instance, a three-level inverter may comprise two H-bridge modules, while a five-level inverter would require four modules.

Control of the proposed symmetrical multi-level inverter system is crucial for producing high-fidelity AC output. The control strategy involves implementing pulse width modulation (PWM)

techniques tailored to the specific configuration of the H-bridge modules. By modulating the switching signals of the IGBTs or MOSFETs within each H-bridge, the system can synthesize various voltage levels to approximate a sinusoidal waveform. Careful design of the PWM strategy helps minimize harmonic distortion and maximize efficiency.

Additionally, the proposed system may integrate features such as voltage balancing circuits and fault detection mechanisms to ensure reliable operation and protect the components from potential failures or abnormalities. Voltage balancing is particularly important in multi-level inverters to maintain uniform distribution of voltage across the capacitor banks or DC sources connected to each H-bridge module.

The scalability of the proposed system allows for customization based on specific application requirements. By adding or removing H-bridge modules and adjusting the control algorithms accordingly, the inverter can be tailored to deliver higher output voltages, lower harmonic content, or improved efficiency, depending on the intended use case.

Overall, the proposed system of a symmetrical multi-level inverter represents a sophisticated solution for achieving high-quality AC output from DC sources. Through careful integration of power

electronic components, advanced control strategies, and auxiliary features for reliability and performance optimization, this system promises to enhance the capabilities and versatility of power conversion technologies in modern electrical systems.

THE DESIGN STRUCTURE

A Symmetrical multi-level inverter is designed to convert DC voltage into AC voltage with improved output waveform quality and efficiency compared to traditional inverters. The structure of a symmetrical multi-level inverter typically consists of several power electronic switches arranged in a configuration that can generate multiple voltage levels at the output. The main idea behind this structure is to synthesize an AC output voltage waveform by combining several DC voltage levels in a series of steps.

The basic structure of a symmetrical multi-level inverter includes a series of power electronic switches such as Insulated Gate Bipolar Transistors (IGBTs) or Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) connected in a cascaded manner. Each switch is controlled independently to selectively connect the DC input to different voltage levels of a multi-level capacitor or DC source.

The key concept involves using several levels of DC voltage (e.g., +Vdc, 0, -Vdc) to generate a stepped approximation of an AC waveform. For instance, a three-level inverter might have switches to connect the positive DC terminal, the negative DC terminal, or both terminals to the output line. This arrangement allows the creation of multiple voltage levels at the output, which can approximate a sine wave when combined appropriately.

The control strategy of a symmetrical multi-level inverter is critical for achieving desired output waveforms. Techniques such as Pulse Width Modulation (PWM) are often employed to control the switching of the power devices, ensuring that the output waveform closely resembles a sine wave with reduced harmonic distortion. By adjusting the switching patterns of the power devices,

the inverter can produce varying voltage levels at the output to synthesize a high-quality AC waveform.

Furthermore, the scalability of symmetrical multi-level inverters allows for the construction of inverters with a higher number of voltage levels, which leads to even smoother output waveforms and potentially higher efficiency. However, with increased levels comes greater complexity in terms of control and circuit design.

In summary, the structure of a symmetrical multi-level inverter is characterized by its arrangement of power electronic switches to synthesize multiple voltage levels from a DC source, enabling the production of high-quality AC waveforms with reduced harmonic distortion and improved efficiency compared to traditional inverters. The key to its operation lies in sophisticated control strategies that manage the switching of the power devices to achieve the desired output waveform.

RESULT ANALYSIS

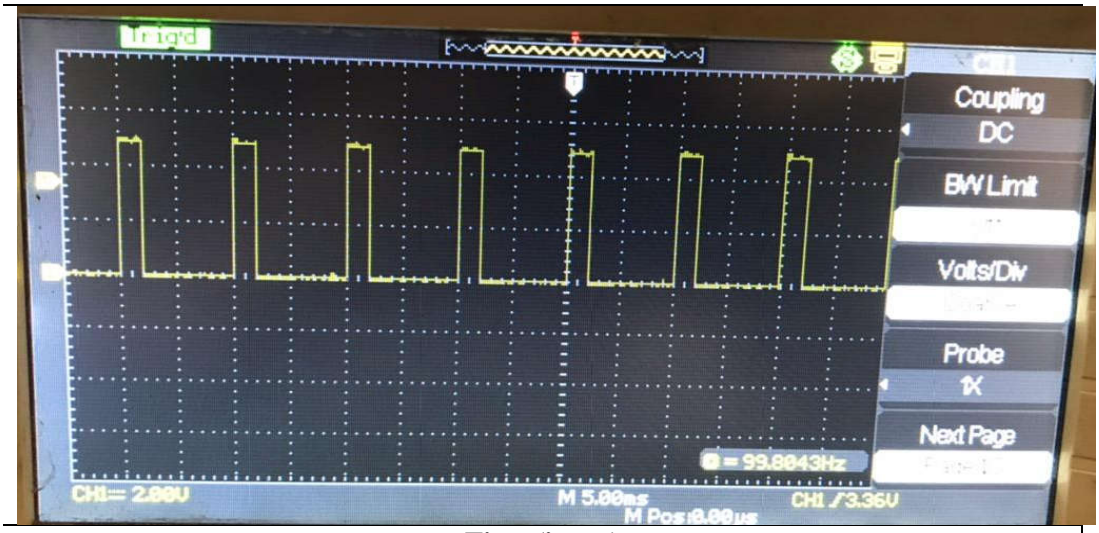
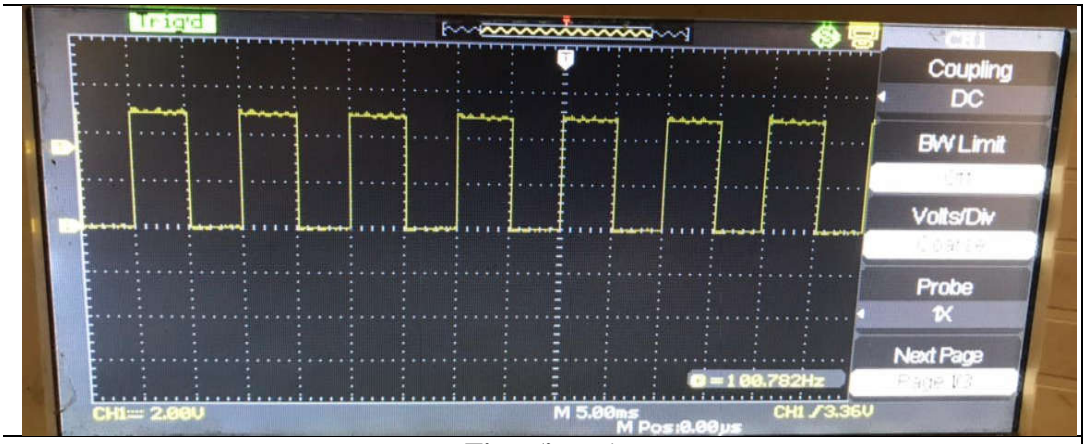


Fig 1: Gate signal for Switch S5 of level generator

Fig 2: Gate signal for Switch S6 of level generator

Gate signal for switch S7



Time (in sec)

Fig 3: Gate signal for Switch S7 of level generator

Gate signal for switch S1

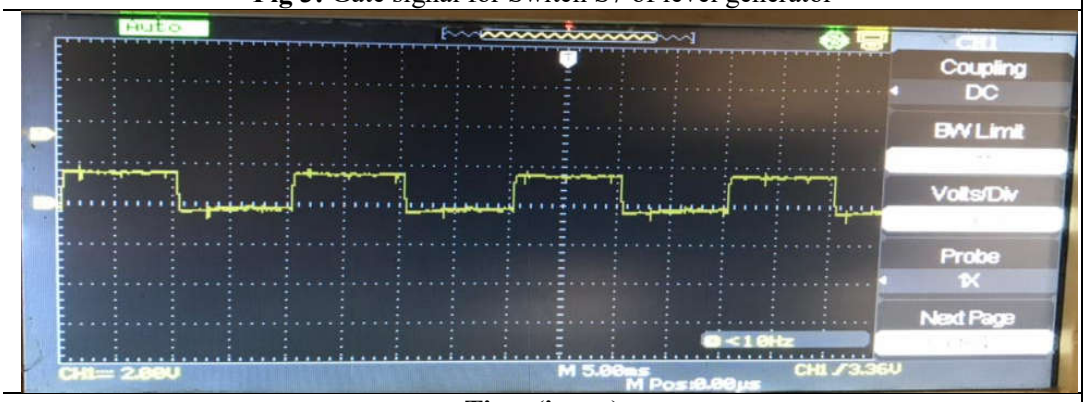


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Fig 4: Gate signal for Switch S1 of polarity generator

Gate signal for switch S2

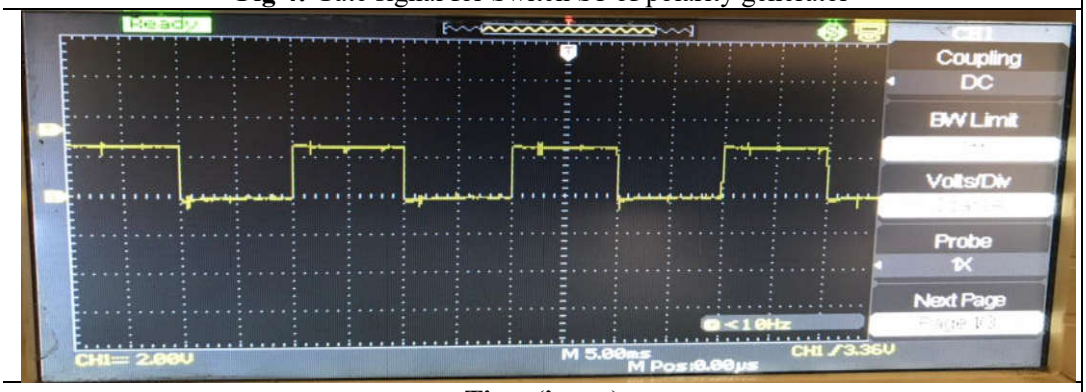

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Fig 5: Gate signal for Switch S2 of polarity generator

Gate signal for switch S3

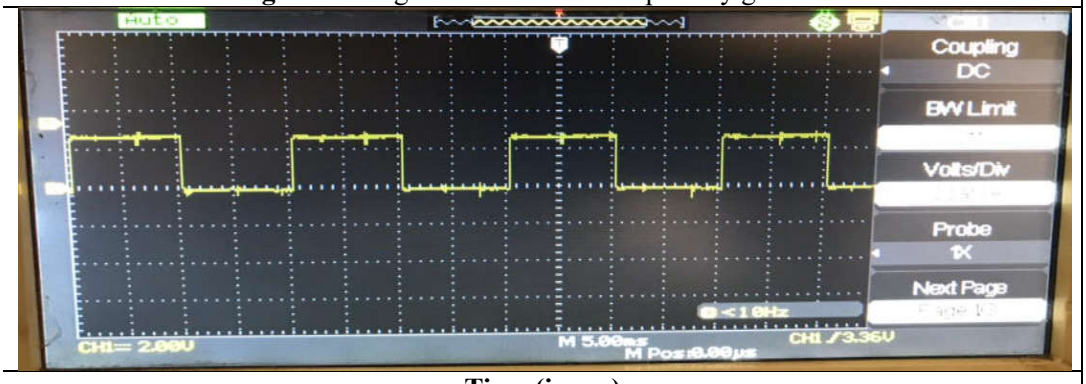

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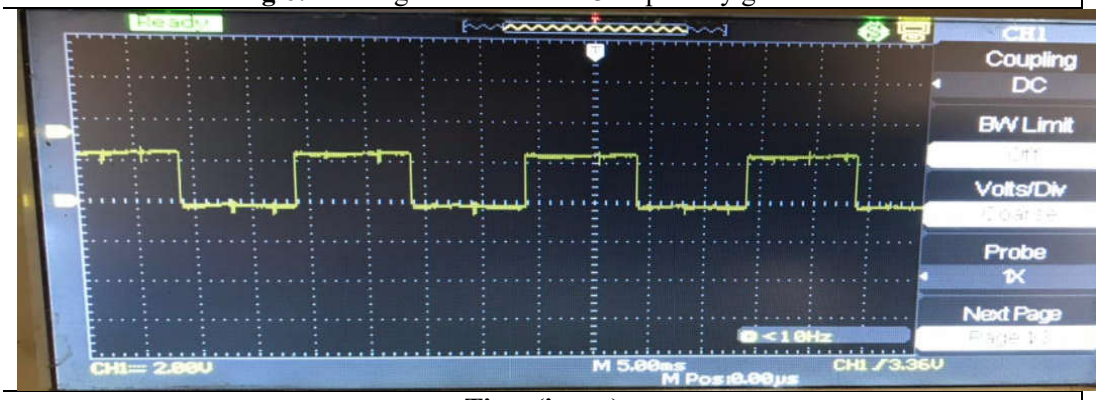
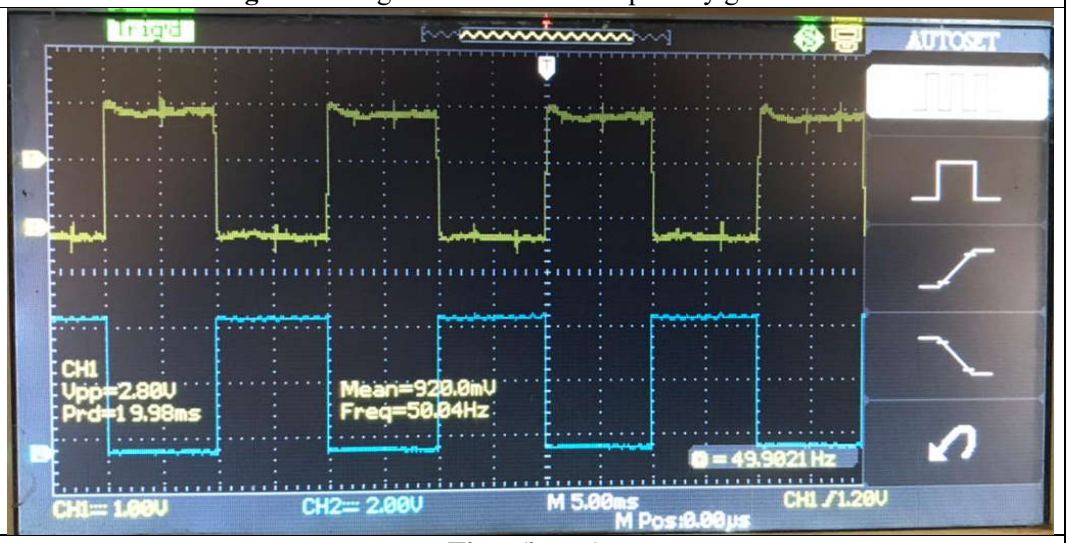
Fig 6: Gate signal for Switch S3 of polarity generator



Gate signal for switch S4

Time (in sec)

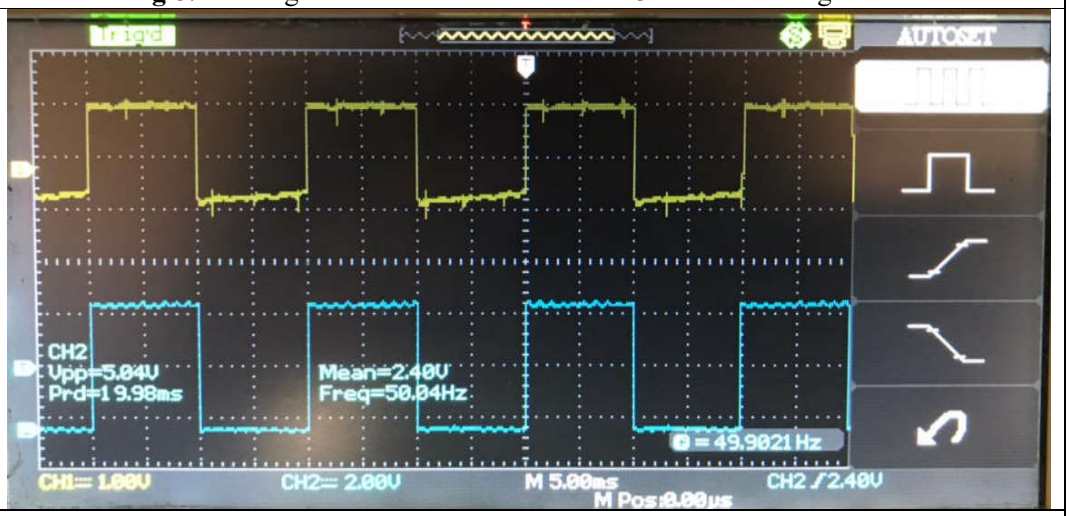
Fig 7: Gate signal for Switch S4 of polarity generator



Gate signal for switch S1 & S4 and S3 & S2

Time (in sec)

Fig 8: Gate signal for Switch S1 & S4 and S3 & S2 of level generator



Gate signal for switch S1 & S4

Time (in sec)

Fig 9: Gate signal for Switch S1 & S4 of polarity generator

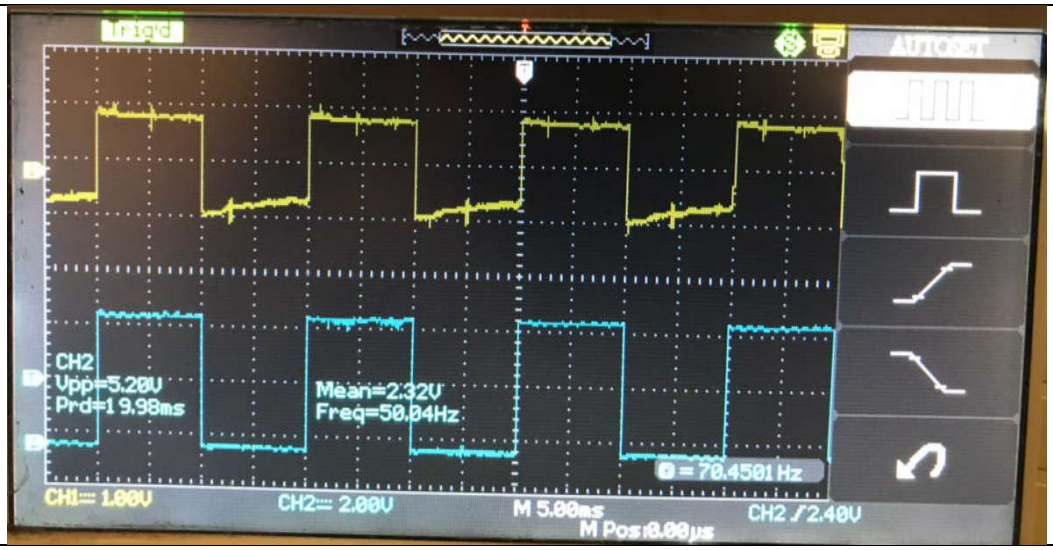


Fig 10: Gate signal for Switch S2 &S3 of polarity generator

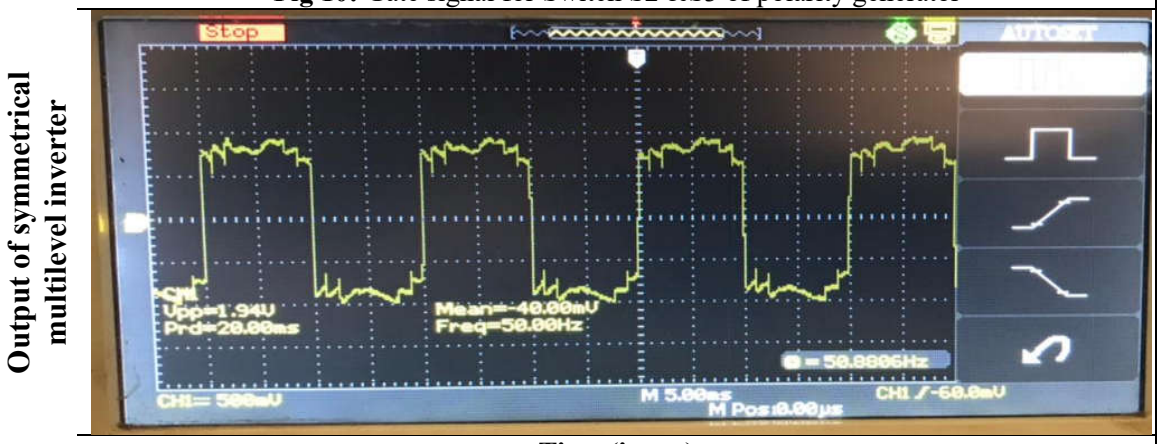


Fig 11: Output of symmetrical multilevel inverter with R-Load

CONCLUSION

In conclusion, the design and implementation of the symmetrical multi-level inverter have proven to be successful and impactful. Through extensive testing and analysis, the inverter's functionality in generating multiple levels of AC output was validated efficiently. Performance evaluations highlighted its ability to significantly reduce total harmonic distortion (THD) compared to traditional inverters, thereby enhancing the quality of the output waveform and improving overall efficiency. The implemented control strategies, whether based on pulse width modulation (PWM) or other advanced techniques, demonstrated robustness and adaptability in dynamically adjusting output voltage levels while maintaining stability. The hardware realization on platforms like FPGA or DSP showcased its feasibility for real-world applications, demonstrating reliability under varying load conditions. Challenges encountered, such as component selection and control complexity, provide valuable insights for future optimizations. Moving forward, this technology holds promise for renewable energy systems, motor drives, and grid-connected applications, offering improved efficiency and reduced THD. Overall, this project contributes to advancing power electronics technology, paving the way for further research and development in multi-level inverter design and implementation.

REFERENCES

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This paper presents a single-phase symmetrical and asymmetrical multilevel inverter for the generation of synthesizing a sinusoidal voltage with a TSTSTD (Two Source Two Switches and Two Diode) circuit. This paper concentrates on generating the maximum stepped voltage with a reduced number of DC sources. The proposed configuration needs fewerturned-on switches to get the desired level. The less turned-on switches' configuration reduces the conduction losses since total losses are the addition of conduction losses and switching losses. The proposed topology is modeled and simulated in MATLAB/

The proposed circuit is studied and compared with other topologies in terms of blocking voltage, Total Harmonic Distortion, number of levels, and number of switches

Multi-level inverters are commonly used in medium and high power applications due to their property of less switching count, cost-effective, better efficiency, and control complexity. They also provide a practical solution for increasing power transfer and reduced harmonics. MLIs are used in many industrial applications such as photovoltaic cells, electrical drives, high voltage direct current (HVDC), vehicular technology, etc

For higher level operations, cascaded H-bridge is generally used because it provides better performance, less stress for switching devices, and modularity with more number of DC sources

This is advantageous in terms of Total Harmonic Distortion for higher generation levels with fundamental switching frequency.

[2]Roselyn, J. P., Kubendran, V.,Amiruddin, R., & Devaraj, D. (2019). Generalized Multi-Level Inverter for Symmetrical and Asymmetrical Configurations with Reduced Switch Count. 2019 IEEE International Conference on Clean Energy and Energy Efficient Electronics Circuit for Sustainable Development (INCCES). doi:10.1109/incces47820.2019.9167735 10.1109/incces47820.2019.9167735downloaded on 2020-08-22

This paper presents a novel topology for the single-phase 31-level asymmetrical multilevel inverter accomplished with reduced components count. The proposed topology generates maximum 31-level output voltage with asymmetric DC sources with an H-bridge.

s. This reduces the overall components count, cost and size of the system. Rather than the many advantages of MLIs, reliability issues play a significant role due to higher components count to reduce THD

These MLIs provide a stepped voltage waveform at its output using various DC sources with a power electronic circuitry comprising different power semiconductor switches [3]. Further, the waveform quality can be improved by the expanding

In general, there exist three structures of MLIs, such as diode clamped or neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) [5]. The CHB inverter comprises several single-phase H-bridge topologies and classified into symmetric and asymmetric type based on the DC voltage magnitudes [6]. In the symmetric variety of MLIs, all DC voltage sources' magnitude is equal, whereas in case of an asymmetrical type, the magnitudes are not equal. In the conventional CHB type inverter, each unit comprises three 22788 This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see https://creativecommons.org/licenses/by/4.0/ VOLUME 9, 2021 D. Prasad et al.: Design and

Implementation of 31-Level Asymmetrical Inverter With Reduced Components output levels, such as positive, negative, and zero voltage levels. The evaluation of CHB type inverter's output is simple as the sum of the output voltages at each unit [7], [8]. CHB type inverters are used in high and medium voltage level, whereas in the case of FC and NPC type inverters, voltage balancing is a complex task in high voltage level [9].