A FIR FILTER'S EFFICIENT VLSI DESIGNING APPROACH BASED ON FIXED COEFFICIENT RNS

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ABSTRACT
In this work, a residue number system (RNS)-based fixed coefficient finite impulse response filter implementation is provided for the moduli set of 2k-1, 2k, and 2k+1. By employing a pre-loaded product block, the novel multiplication method lowers the number of incomplete products. In comparison to the traditional modular multiplication, the suggested modular multiplication enhances clock frequency while using less area and power due to the reduction in partial products. Moreover, the current method does away with the necessity for a circuit that converts binary numbers to residue numbers, which is often required at the front end of RNS-based systems. Two fixed coefficient filter topologies using the novel modular multiplication technique are given in this paper. Performance comparison shows that the proposed structure involves significantly less ADP and less EPS than the existing block direct-form structure for medium or large filter lengths while for the short-length filters, the existing block direct-form structure has less ADP and less EPS thanthe proposed structure. Application-specific integrated circuit synthesis result shows that the proposed structure for block size 4 and filter length 64 involve 42% less ADP and 40% less EPS than the best available FIR filter structure of for reconfigurable applications. For the same filter length and the same block size, the proposed structure involves 13% less ADP and 12.8% less EPS than that of the existing direct-from blocks FIR structure.

INTRODUCTION
Finite impulse response (FIR) filters are favored over infinite impulse response (IIR) filters in many digital signal processing systems, including telephony and audio-video systems, since they are stable and always have a linear phase response. In the FIR filter transfer function, stability and linear phase response are produced by the presence of only zeros and symmetric filter coefficients, respectively. In higher clock frequency applications, the transposed direct form (TDF) FIR filter structure is recommended over the direct form (DF) filter architecture (Parhi, 2007). Due to the simultaneous arithmetic operations with tiny size residue numbers, the clock frequency may also be increased utilizing RNS-based FIR filter structures. A binary number is represented in RNS by a series of digits starting with { 1 m, 2 m , 3 m ..., q m } called moduli (P. V. A. Mohan, 2002). Here, q represents the number of modulus presented in a moduli set. These modulus values are relatively prime to each other. The dynamic range is defined as [0,M −1] for a given moduli set. Here M is the maximum number of a given moduli set and is defined in equation (1). The residues of any number between 0 to M −1 are represented uniquely for a given moduli set (P. V. A. Mohan, 2002). The RNS-based FIR filters are implemented with forward converter (for binary to residue conversion), arithmetic circuits such as modulo multipliers and modulo adders for each modulus and a reverse converter (for residue to binary conversion). In the past, several FIR filter implementations were reported using RNS (Jenkins & Leon, 1977; Wheaton & Current, 1982; Bayoumi, Jullien, & Miller, 1985; Soder-strand & Escott, 1986; Pardikar, Tummala, & Rao, 1987; C.-L. Wang, 1994; Conway, 2006; Zivaljevic, Stamenkovic, & Stojanovic, 2012; Vun, Premkumar, & Zhang, 2013). All these filters are implemented using {2k −1,2k ,2k +1} moduli set. The modulo multiplication and addition of 2k +1 modulus requires more hardware as compared to 2k −1 and 2k modulus. Also, modulo multiplication by powers of 2 is not as simple as left circular rotation in a 2k −1 modulus (Hiasat & Abdel, 1998). Hence, we considered {2k −1,2k ,2k• }1 −1} moduli sets for the filter implementations. In (S. Kotha, Singhvi, & Sahoo, 2013), filters are implemented with {2k −1,2k ,2k−1 −1}. FIR: It implies Finite Impulse Response Filter
We realize that consider computerized channels whose motivation reaction is of limited of length, so

these channels are properly alluded to as limited drive reaction (FIR) digitals channels. In this way, if the yield tests of the framework depend just on the present info, and a limited number of past information tests, at that point the channel has a limited motivation reaction as appeared in Figure 1.3.

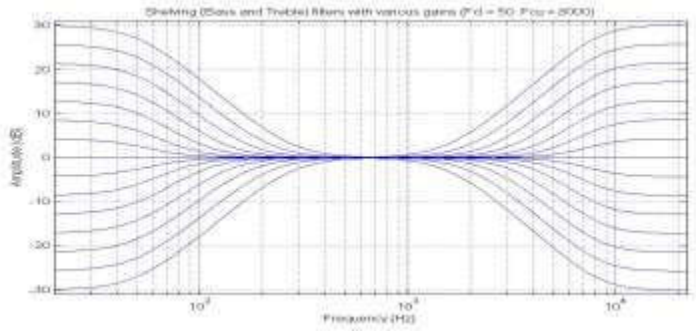


Figure 1: Relation between frequency and the amplitude

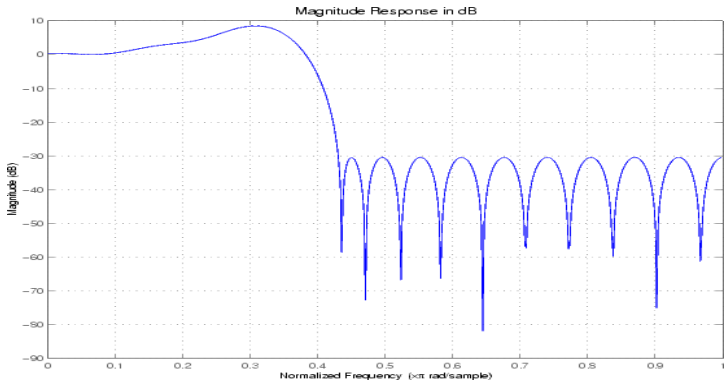


Figure 2: FIR Digital Filters

Characteristics of FIR digital filters Some preferred standpoint and hindrance of FIR channels contrasted with their IIR partners are:

1. FIR channels can be outlined with precisely direct stage. Straight stage critical for applications where stage twisting because of nonlinear stage can corrupt execution, for instance, discourse preparing, information transmission and relationship handling
2. FIR channels understood no recursively are innately steady, that is, the channel motivation reaction is of limited length and there for reinforced.
3. Quantization clamor because of limited exactness number juggling can be made immaterial for no recursive acknowledge.
4. Coefficient exactness issues inalienable in sharp cut off IIR channels can be made less serious for acknowledge of similarly sharp FIR channel
5. FIR channels can be productively executed in multi rate frameworks.
6. A weakness of FIR channels contrasted with IIR channels is that an obviously higher request channel is required to accomplish a predetermined greatness reaction, along these lines requiring more channel coefficient stockpiling.

LITERATURE SURVEY

Limited IMPULSE reaction (FIR) computerized channel is generally utilized in a few advanced flag handling applications, for example, discourse preparing, uproarious speaker evening out, resound scratch-off, versatile commotion crossing out, and different correspondence applications, including programming characterized radio (SDR) et cetera [1]. Huge numbers of these applications require FIR channels of vast request to meet the stringent recurrence details [2]– [4].Very regularly these channels need to help high testing rate for rapid advanced correspondence [5]. The quantity of augmentations and increments required for each channel yield, in any case, increments straightly with the channel arrange. Since there is no repetitive calculation accessible in the FIR channel calculation, ongoing usage of an extensive request FIR channel in an asset compelled condition is a testing assignment. Channel

coefficients frequently stay steady and known from the earlier in flag preparing applications. This component has been used to diminish the multifaceted nature of acknowledgment of increases. A few outlines have been proposed by different specialists for proficient acknowledgment of FIR channels (having settled coefficients) utilizing dispersed number juggling (DA) [18] and various consistent augmentation (MCM) techniques [7], [11]–[13]. DA-based outlines utilize query tables (LUTs) to store precomputed results to lessen the computational multifaceted nature. The MCM technique then again decreases the quantity of increases required for the acknowledgment of duplications by normal subexpression sharing, when a given info is duplicated with an arrangement of constants. The MCM plot is more powerful, when a typical operand is duplicated with more number of constants. In this manner, the MCM plot is reasonable for the execution of substantial request FIR channels with settled coefficients. Be that as it may, MCM squares can be shaped just in the transpose frame arrangement of FIR channels. Square handling strategy is prominently used to determine high-throughput equipment structures. It gives throughput-versatile plan as well as enhances the zone postpone effectiveness. The induction of square based FIR structure is clear when coordinate frame setup is utilized [16], while the transpose shape arrangement does not specifically bolster square preparing. Be that as it may, to take the computational favorable position of the MCM, FIR channel is required to be acknowledged by transpose shape setup. Aside from that, transpose frame structures are intrinsically pipelined and expected to offer higher working recurrence to help higher testing rate. There are a few applications, for example, SDR channelizer, where FIR channels should be executed in a reconfigurable equipment to help multistandard remote correspondence [6]. A few plans have been proposed amid the most recent decade for proficient acknowledgment of reconfigurable FIR (RFIR) utilizing general multipliers and consistent duplication plans [7]– [10]. A RFIR channel design utilizing calculation sharing vector-scaling method has been proposed in [7]. Chen and Chiueh [8] have proposed a canonic sign digit (CSD)- based RFIR channel, where the nonzero CSD esteems are altered to diminish the accuracy of channel coefficients without critical effect on channel conduct. However, the reconfiguration overhead is altogether huge and does not give a zone postpone effective structure. The designs in [7] and [8] are more proper for bring down request channels and not reasonable for channel channels because of their vast zone complexity.Constant move technique (CSM) and programmable move strategy have been proposed in [9] for RFIR channels, particularly for SDR channelizer. As of late, Park and Meher [10] have proposed a fascinating DA-based design for RFIR filter.The existing multiplier-based structures utilize either directform arrangement or transpose frame setup. Be that as it may, the multiplier-less structures of [9] utilize transpose frame arrangement, though the DA-based structure of [10] utilizes coordinate shape setup. In any case, we don't locate a particular square based plan for RFIR channel in the writing. A square based RFIR structure can without much of a stretch be inferred utilizing the plan proposed in [15] and [16]. In any case, we find that the square structure acquired from [15] and [16] isn't effective for substantial channel lengths and variable channel coefficients, for example, SDR channelizer. Consequently, the plan strategies proposed in [15] and [16] are more appropriate for 2-D FIR channels and square minimum mean square versatile channels. In this, we investigate the likelihood of acknowledgment of square FIR channel in transpose frame setup with a specific end goal to exploit the MCM plans and the inborn pipelining for region postpone effective acknowledgment of expansive request FIR channels for both settled and reconfigurable applications. The fundamental commitments of this paper are as per the following. 1) Computational investigation of transpose shape arrangement of FIR channel and induction of stream diagram for transpose frame square FIR channel with decreased enroll many-sided quality. 2) Block plan for transpose shape FIR channel. 3) Design of transpose frame square channel for reconfigurable applications. 4) A low-multifaceted nature outline strategy utilizing MCM conspire for the square usage of settled FIR channels. The rest of this paper is composed as takes after. In Section II, computational investigation and scientific definition of square transpose shape FIR channel are displayed. The proposed structures for settled and reconfigurable applications are introduced in Section III. Equipment and time complexities alongside execution correlation are introduced in Section IV. At last, the end is attracted Section V.

PROPOSED SYSTEM

PROPOSED STRUCTURES

Transpose form finite-impulse response (FIR) filters are inherently pipelined and support multiple constant multiplications (MCM) technique that results in significant saving of computation. However, transpose form configuration does not directly support the block processing unlike directform configuration. In this paper, we explore the possibility of realization of block FIR filter in transpose form configuration for area-delay efficient realization of large order FIR filters for both fixed and reconfigurable applications. Based on adetailed computational analysis of transpose form configuration of FIR filter, we have derived a flow graph for transpose form block FIR filter with optimized register complexity. Ageneralized block formulation is presented for transpose form FIR filter. We have derived a general multiplier-based architecture for the proposed transpose form block filter for reconfigurable applications. A low-complexity design using the MCM scheme is also presented for the block implementation of fixed FIR filters. The proposed structure involves significantly less areadelay product (ADP) and less energy per sample (EPS) than the existing block implementation of direct-form structure for medium or large filter lengths, while for the short-length filters, the block implementation of direct-form FIR structure has less ADP and less EPS than the proposed structure. Applicationspecific integrated circuit synthesis result shows that the proposed structure for block size 4 and filter length 64 involves 42% less ADP and 40% less EPS than the best available FIR filter structure proposed for reconfigurable applications. For the same filter length and the same block size, the proposed structureinvolves 13% less ADP and 12.8% less EPS than that of the existing direct-form block FIR structure. FINITE-IMPULSE response (FIR) digital filter is widely used in several digital signal processing applications, such as speech processing, loud speaker equalization, echo cancellation, adaptive noise cancellation, and various communication applications, including software-defined radio (SDR) and so on [1]. Many of these applications require FIR filters of large order to meet the stringent frequency specifications [2]–[4]. Very often these filters needto support high sampling rate for high-speed digital communication [5]. The number ofmultiplications and additions required for each filter output, however, increases linearly with the filter order. Since there is no redundant computation available in the FIR filter algorithm, real-time implementation of a large order FIR filter in a resource constrained environment is a challenging task. Filter coefficients very often remain constant and known a priori in signal processing applications. This feature has been utilized to reduce the complexity of realization of multiplications. Several designs have been suggested by various researchers for efficient realization of FIR filters (having fixed coeffi- cients) using distributed arithmetic (DA) [18] and multiple constant multiplication (MCM) methods [7], [11]–[13]. DA-based designs use lookup tables (LUTs) to store precomputed results to reduce the computational complexity. The MCM method on the other hand reduces the number of additions required for therealization of multiplications by common subexpression sharing, when a given input is multiplied with a set of constants. The MCM scheme is more effective, when a common operand is multiplied with more number of constants. Therefore, the MCM scheme is suitable for the implementation of large order FIR filters with fixed coefficients. But, MCM blockscan be formed only in the transpose form configuration of FIR filters. Block-processing method is popularly used to derive high-throughput hardware structures. It not only provides throughput-scalable design but also improves the area-delay efficiency. The derivation of block-based FIR structure is straightforward when direct-form configuration is used [16], whereas the transpose form configuration does not directly support block processing. But, to take the computational advantage of the MCM, FIR filter is required to be realized by transpose form configuration. Apart from that, transpose form structures are inherently pipelined and supposed to offer higher operating frequency to support higher sampling rate. There are some applications, such as SDR channelizer, where FIR filters need to be implemented in a reconfigurable hardware to support multistandard wireless communication [6]. Several designs have been suggested during the last decade for efficient realization of reconfigurable FIR (RFIR) using general multipliers and constant multiplication schemes [7]– [10]. A RFIR filter architecture using computation sharing vector-scaling technique has been proposed in [7]. Chen and Chiueh [8] have proposed a canonic sign digit

(CSD)-based RFIR filter, where the nonzero CSD values are modified to reduce the precision of filter coefficientswithout significant impact on filter behavior. But, the reconfiguration overhead is significantly large and does not provide an area-delay efficient structure. The architectures in [7] and [8]are more appropriate for lower order filters and not suitable for channel filters due to their large area complexity. Constant shift method (CSM) and programmable shift method.

FIR filters are digital filters with finite impulse response. They are also known as non- recursive digital filters as they do not have the feedback (a recursive part of a filter), even though recursive algorithms can be used for FIR filter realization.

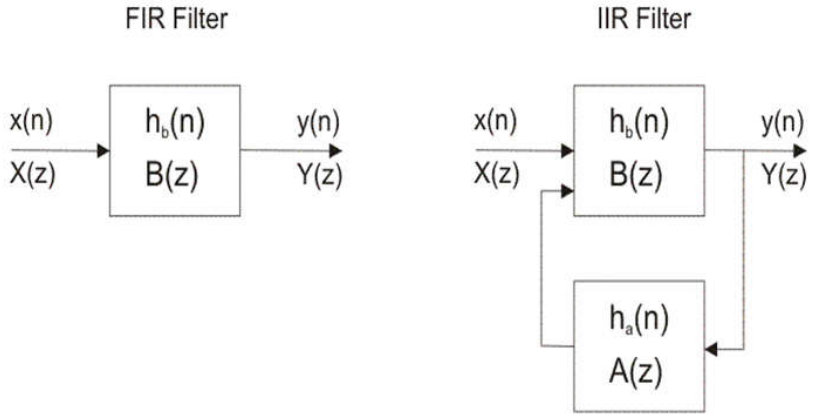


Figure 3:. Block diagrams of FIR and IIR filters

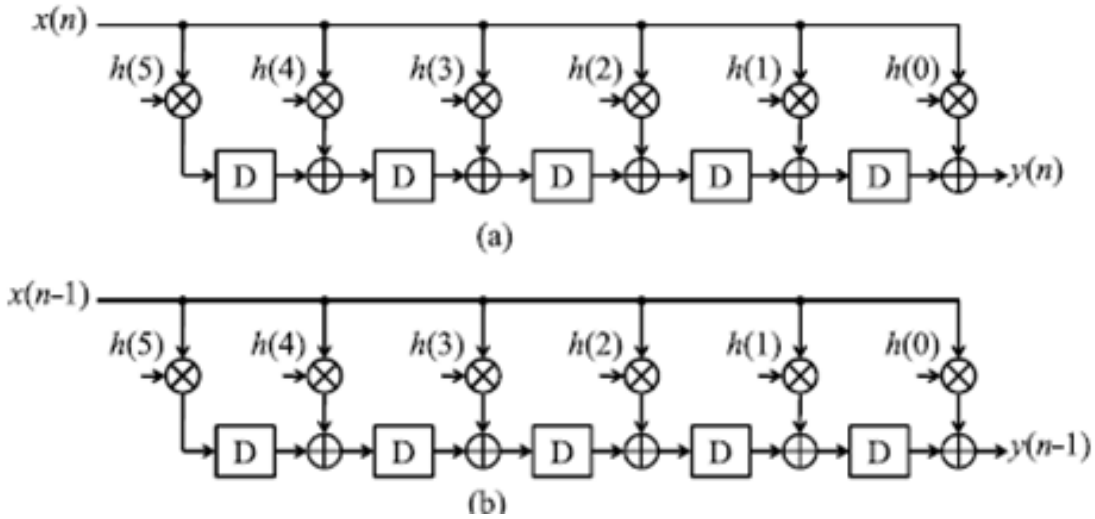
FIR filters can be designed using different methods, but most of them are based on ideal filter approximation. The objective is not to achieve ideal characteristics, as it is impossible anyway, but to achieve sufficiently good characteristics of a filter. The transfer function ofFIR filter approaches the ideal as the filter order increases, thus increasing the complexity and amount of time needed for processing input samples of a signal being filtered.

MATHEMATICAL FORMULATION OF BLOCK TRANSPOSE FORM FIR FILTER

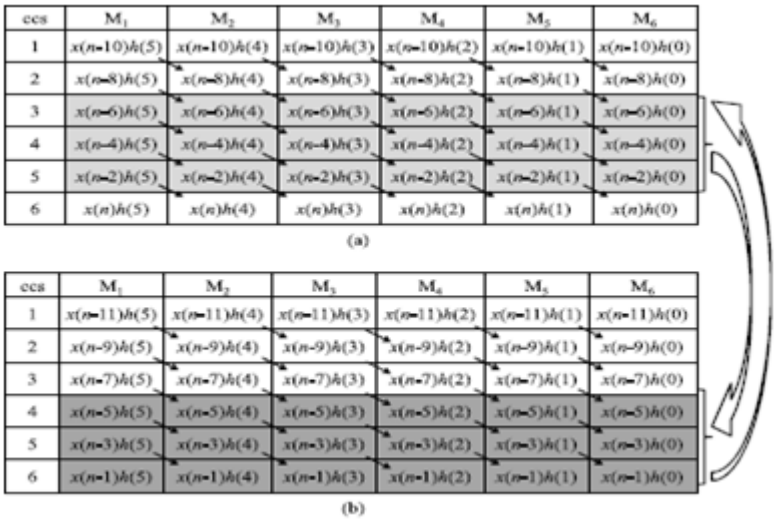
$$y(n) = \sum_{i=0}^{N-1} h(i) \cdot x(n-i). \qquad (1)$$

$$Y(z) = [z^{-1}(\cdots(z^{-1}(z^{-1}h(N-1) + h(N-2)) + h(N-3)) \cdots + h(1)) + h(0)]X(z). \qquad (2)$$

2.2.1 Computational Analysis



2 DFG Transformations



ccs	M_1	M_2	M_3	M_4	M_5	M_6
1	$x(n-10)h(5)$	$x(n-10)h(4)$	$x(n-10)h(3)$	$x(n-10)h(2)$	$x(n-10)h(1)$	$x(n-10)h(0)$
2	$x(n-8)h(5)$	$x(n-8)h(4)$	$x(n-8)h(3)$	$x(n-8)h(2)$	$x(n-8)h(1)$	$x(n-8)h(0)$
3	$x(n-6)h(5)$	$x(n-6)h(4)$	$x(n-6)h(3)$	$x(n-6)h(2)$	$x(n-6)h(1)$	$x(n-6)h(0)$
4	$x(n-4)h(5)$	$x(n-4)h(4)$	$x(n-4)h(3)$	$x(n-4)h(2)$	$x(n-4)h(1)$	$x(n-4)h(0)$
5	$x(n-2)h(5)$	$x(n-2)h(4)$	$x(n-2)h(3)$	$x(n-2)h(2)$	$x(n-2)h(1)$	$x(n-2)h(0)$
6	$x(n)h(5)$	$x(n)h(4)$	$x(n)h(3)$	$x(n)h(2)$	$x(n)h(1)$	$x(n)h(0)$

(a)

ccs	M_1	M_2	M_3	M_4	M_5	M_6
1	$x(n-11)h(5)$	$x(n-11)h(4)$	$x(n-11)h(3)$	$x(n-11)h(2)$	$x(n-11)h(1)$	$x(n-11)h(0)$
2	$x(n-9)h(5)$	$x(n-9)h(4)$	$x(n-9)h(3)$	$x(n-9)h(2)$	$x(n-9)h(1)$	$x(n-9)h(0)$
3	$x(n-7)h(5)$	$x(n-7)h(4)$	$x(n-7)h(3)$	$x(n-7)h(2)$	$x(n-7)h(1)$	$x(n-7)h(0)$
4	$x(n-5)h(5)$	$x(n-5)h(4)$	$x(n-5)h(3)$	$x(n-5)h(2)$	$x(n-5)h(1)$	$x(n-5)h(0)$
5	$x(n-3)h(5)$	$x(n-3)h(4)$	$x(n-3)h(3)$	$x(n-3)h(2)$	$x(n-3)h(1)$	$x(n-3)h(0)$
6	$x(n-1)h(5)$	$x(n-1)h(4)$	$x(n-1)h(3)$	$x(n-1)h(2)$	$x(n-1)h(1)$	$x(n-1)h(0)$

(b)

The calculation of DFT-3 and DFT-4 can be acknowledged by DFG-3 of nonoverlapping obstructs, as appeared in Fig. 4. We allude it to square transpose frame compose I setup of square FIR channel. The DFG-3 can be retimed to get the DFG-4 of Fig.3. 5, which is alluded to square transpose frame compose II arrangement. Note that both sort I and sort II designs include a similar number of multipliers and adders, however type-II setup includes almost L times less postpone components than those of sort I arrangement. We have, in this way, utilized square transpose frame compose II setup to determine the proposed structure. In Section II-C, we present numerical definition of square transpose frame compose II FIR channel for a summed up detailing of the idea of square based calculation of transpose shape FIR filers. Fig.4: DFT of DFG-1 and DFG-2 for three nonoverlapped input blocks [x(n), x(n−1)], [x(n−2), x(n−3)], and [x(n−4), x(n−5)]. (a) DFT-3 for computation of output y(n). (b) DFT-4 for computation of output y(n − 1).

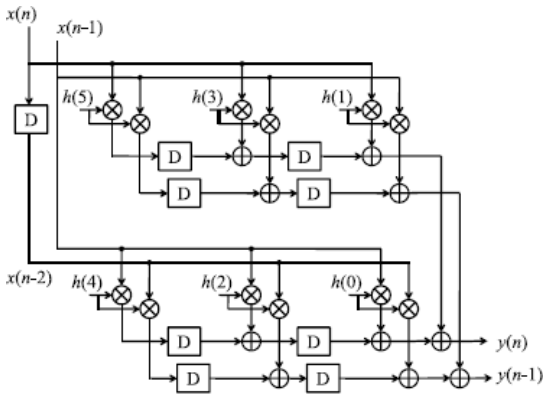


Fig.5: Merged DFG (DFG-3: transpose form type-I configuration for block FIR structure).

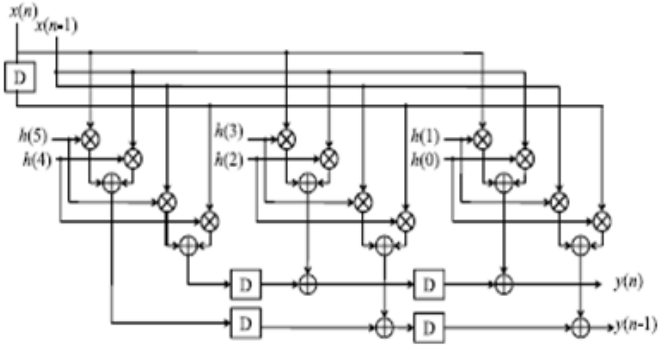


Fig.6: DFG-4 (retimed DFG-3) transpose form type-II configuration for block FIR structure.

SIMULATION RESULTS AND DISCUSSION

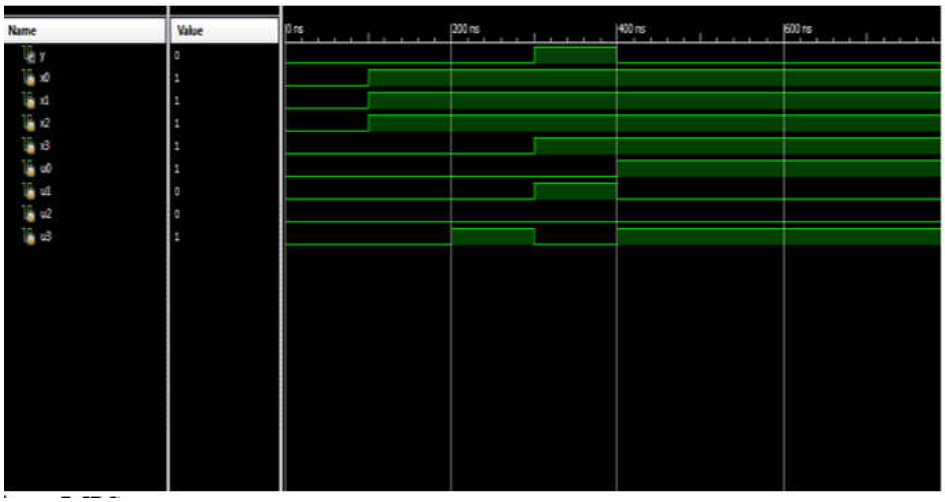


Figure.7 :IPC output

Fig.8: ipu output

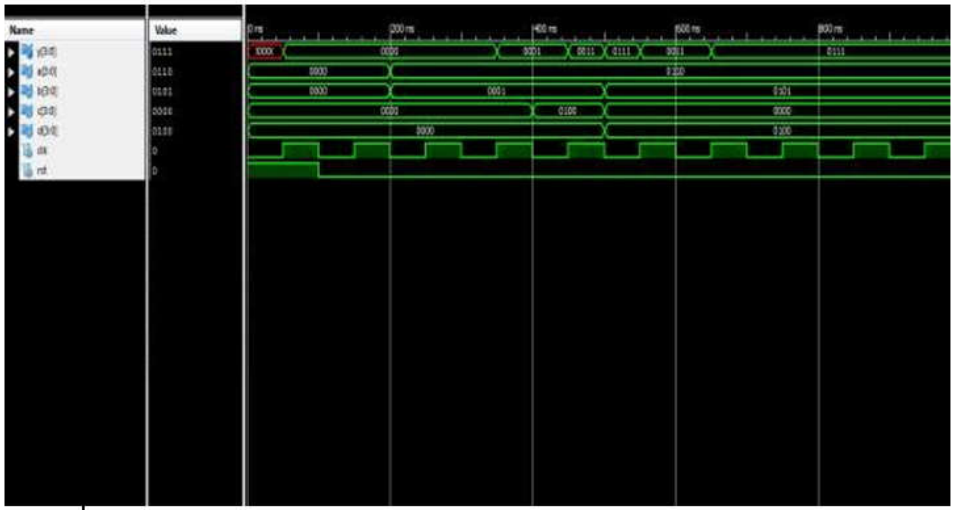


Fig 9: pau output

Fig 10: ru output

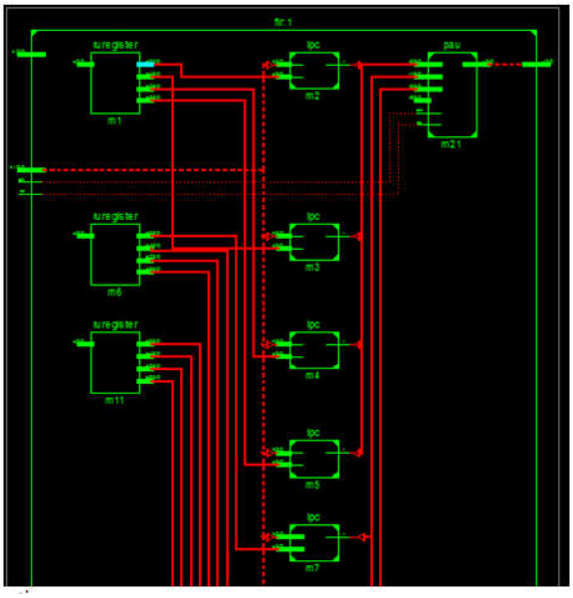


Figure 11: Rtl schematic

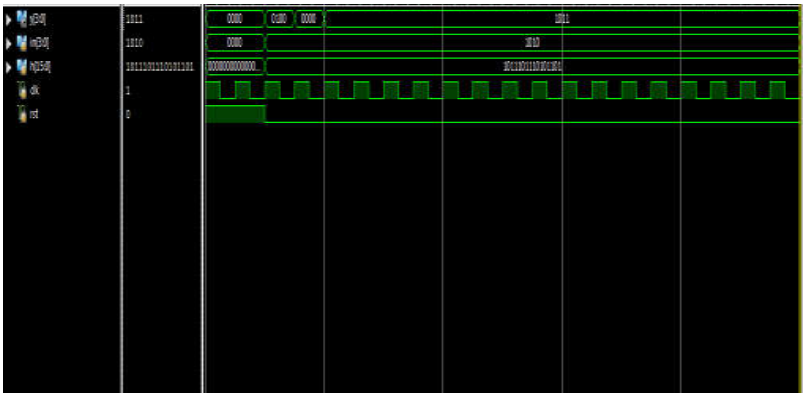


Figure 12: Filter coefficient output Figure 19. CINA

CONCLUSION

In this it is explored the possibility of realization of block FIR filters in transpose form configuration for area delay efficient realization of both fixed and reconfigurable applications. A generalized block formulation is presented for transpose form block FIR filter, and based onthat we have derived transpose form block filter for reconfigurable applications. We have presented a scheme to identify the MCM blocks for horizontal and vertical sub expression elimination in the proposed block FIR filter for fixed coefficients to reduce the computational complexity The filters are implemented using Verilog hardware description language. The United Microelectronics Corporation 90 nm technology library has been used for synthesis and the results area, power and delay are obtained with the help of Cadence register transfer level compiler. The power delay product (PDP) is also considered for performance comparison among the proposed filters. One of the proposed architecture is found to improve PDP gain by 60.83% as

compared with the filter implemented with conventional modular multiplier. The filters functionality is validated with the help of Altera DSP Builder.

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