DESIGN OF SINGLE-EVENT TOLERANT LATCHES IN CMOS TECHNOLOGY FOR ENHANCED SCAN DELAY TESTING

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ABSTRACT:
Nowadays, single event upstes (SEU) and occurrence of delay faults caused by manufacturing defects are significant problems in hhigh-densityVLSI. Thus, rresearchhave drawn great attention on SEU tolerant design and delay fault testing. In the paper, two novel slave latches paper, and a master latch has been proposed to improve the SEU tolerance of a flip flop in scan delay testing. The main purpose of this design is to solve the problems appearing in previous state-of-the-art latches.Simulation results show that the two proposed slave latches can tolerate partical with charges of more than 1 pc . Furthermore , areas of ck-Q delay and power consumption are also investigated and made comparisons with recent state-of-the-art latches. using DSCH3, MICROWIND TOOLS.

INTRODUCTION:
Nowadays, single event effect (SEE) has become a serious design challenge, which limits the reliability and availability of nanoscale flip-flops (FFs)/latches design. If a single event transient (SET) occurs on the node of the FFs/latches and the width of the pulse is wider than the tolerance of the FFs/latches, the logic value stored in the FFs/latches will flip resulting in a single event upset (SEU). SEUs are also regarded as soft errors because they don’t cause permanent damage. However, in some critical applications, soft errors can be detrimental and crucial.
In addition, as the technology scales, another significant problem has been introduced by manufacturing defects, which is known as delay fault. Researchers have proposed two-pattern testing to detect delay faults in manufacturing testing. Two pattern testing contains three well-known approaches, which are known as launch-off-capture (LoC), launch-off-shift (LOS), and enhanced scan testing. The LoC and Los delay testing methods do not allow providing an arbitrary pair of test vectors to the circuit under test, in other words, they only permit the application of limited final vectors to circuits under test, while enhanced scan testing overcomes this limitation at the cost of a higher area overhead.
To reduce the soft errors produced by SEUs and meanwhile detect delay faults, many FFs/latches designs for testability (DFT) with SEU tolerant capability have been proposed. However, the area overhead of the circuits it is not small, as well as the circuits proposed.The authors proposed two types of (SEU) tolerant FFs that tolerate SEUs and allow enhanced scan delay fault testing. The proposed FFs in are master-slave FFs, and the slave latches are constructed by modifying the existing SEU tolerant latches, namely, the soft error hardened (SEH) latches proposed in. The authors introduce the idea that a slave latch can be divided into two latches during testing, and applied it to the SEH latch. Compared with the latch-in, the proposed two types of the FFs have smaller areas,shorter CK-Q delays, and lower average power consumption. However, as mentioned in, the slave latches proposed in suffer from high impedance states when the strike occurs on their internal nodes, resulting in an undesired leakage. To solve this problem, the authors of proposed two modifying slave latch by adding another four transistors. Though the simulation results show better performances, the circuit proposed also has some problems which will be discussed in detail later in the next sections.
In this paper, a novel master latch and two slave latches are proposed to solve the problem discussed above. The proposed latches have much better performance on SEU tolerant capability; meanwhile, they allow enhanced scan testing.

EXISTING SYSTEM:

Fig. 1 shows the structure of the SEU tolerant FF for enhanced scan testing, which contains a selector, the master and slave latch. The FFs use the SEH latch shown in Fig. 2 as the master latch. Fig. 3 shows the slave latches (referred to as type-I). As mentioned, during system operation, the type-I slave latch operates the same as the SEH latch. According to the value of the clock signal, system operation is further divided into two operation modes: transparent mode (when the clock is "1") and hold mode (when the clock is "0"); during the scan-shift operation, the slave latch is split into two small dynamic latches. The operations of SEH latch and FF have been presented .

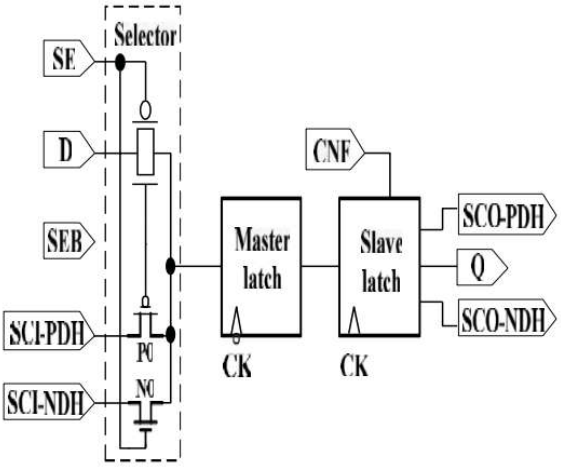

Fig. 1. Structure of the SEU tolerant flip-flop for enhanced scan testing

The type-I slave latch used has an apparent defect. That is, if the width of a SET occurring on node PDH or NDH is larger than the decay time of node DH, a soft error will occur, and it cannot be corrected until new data rewrite this node. For example, if the input signal is "0" in the transparent mode, then during the hold mode, if node PDH becomes "1" due to a SET, node DH is in a highimpedance state which further makes node DHgradually lose its stored charge, resulting in a soft error.

The additional transistors would realize the following function: in transparent mode, for example, if the input signal is "0", then nodes PDH and NDH are "0", node DH is "1", transistors N10 and P11 would be on, N11 and P10 are off. Therefore, DH is connected to Vdd through P1 rather than N11 and N10. If a particle strikes on node PDH during hold mode, node PDH becomes 1 temporarily, P1 is off at the same time, after that, the error occurring on node PDH turns on N11, so node DH would be connected to Vdd through N10 and N11, which would prevent node DH taking into the highimpedance state. Node PDH can be recovered by the correct data stored at nodes NDH and DH through P2 and P3.

However, type-A and type-B slave latches cannot work well as stated, because when PDH is hit by particles, PDH becomes "1", it seems that both transistors N10 and N11 would be turned on. But, in fact, transistors N10 cannot charge node DH. For transistors N10, Vd=Vg-Vth, it means that, during the leakage of node DH, transistors N10 and N11 cannot charge node DH back to "1", which makes the leakage inevitably occur on node DH. In the same way, nodes PDH and NDH store "1", node DH store "0", when node NDH is hit, it is easy can be concluded that node DH cannot be connected to Gnd through transistors P10 and P11. To summarize, the additional four transistors added to type-A and type-B slave latches cannot fulfill their correct function as the authors said, but just increase the capacitances of node DH.

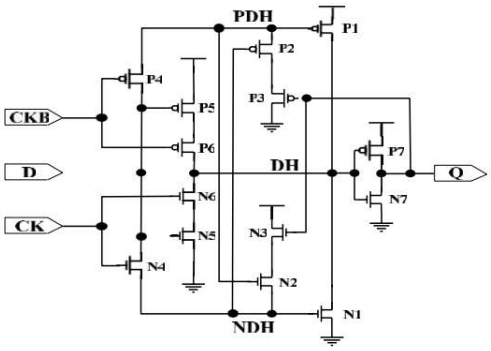

Fig. 2. SEH latch proposed

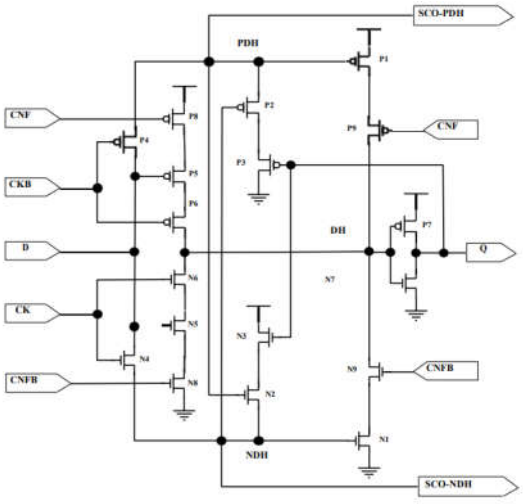

Fig. 3. Slave latch of Type-I SEU tolerant flip-flop

when the latches work on its hold mode, either node PDH or NDH cannot be connected to Vdd or Gnd, leading to high-impedance state and then resulting in leakages.

PROPOSED MASTER LATCH:

Fig. 5 shows the proposed master latch. Compared with the SEH latch, six more transistors P12, P13, P14, N12, N13, and N14 are added to this latch. These additional transistors together with transistors P2, P3, N2, and N3 can guarantee that nodes PDH, NDH, DH as well as the new nodes PD and ND are always connected to either GND or Vdd in hold mode.

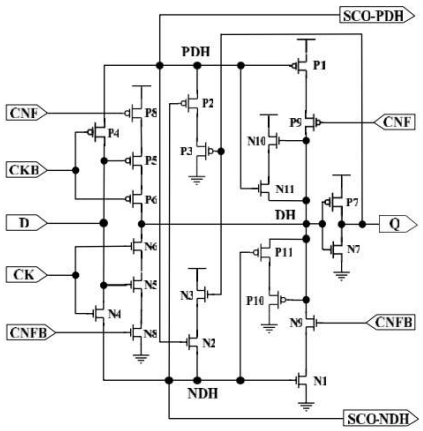

Fig. 4. Slave latch of Type-A SEU tolerant flip-flop

When the clock is high, P4, P6, N4, and N6 are on, and the proposed master latch is in its transparent mode. If the input signal is “1”, the value stored on nodes PDH and NDH is ”1”, then P2, P3, and P13 are off, P12, and N12 are on, PDH is connected to Vdd through P12, and node PD is connected to Gnd through N12.
At the same time, P14 and N14 are off, N2, N3, and N13 are on, node NDH is connected to Vdd through N2 and N3, node ND is connected to Vdd through N13, node DH is driven to “0” through N1.
If the input signal is “0”, the value stored on nodes PDH and NDH is set to”0” through P4 and N4, then P2, P3, and P13 are on, P1 2, and N12 are off, nodePDH is connected to Gnd through P2 and P3 and node PD is connected to Vdd through P13, at the same time, P14, N1,4 andN3 are on, N2 and N13ares off, node NDH is connected to Gnd through N14, and node ND is connected to Gnd through N14, DH is driven to “1” through P1.
When the clock is low, P4, P6, N4, and N6 are off, and the proposed master latch is in its hold mode, according to the above analysis, nodes PD, ND, PDH NDH, and DH are always connected to Vdd and Gnd, respectively.
When particles strike on single node PDH, NDH, or DH, noSEUs occur for the same reason that no SEUs occur on the SEH latch. The detailed behavior of the proposed master latch against SET at single node ND or PD is described as follows. During the hold mode, assuming nodes PDH and NDH store “1”, then nodes PD, ND, and DH store “0”, and node PDH is connected to the Vdd through P12, it means that the error transient on node PDH by leakage current will never occur in our proposed master latch. If node PD is hit by a particle, then node PD would upset to “1”, which makes P12 turn off, however, it doesn’t affect nodes NDH, PDH, and DH. If node ND is hit by a particle, then ND would upset to “1”, N14 turns on, NDH can be pulled down, P1 turn off, however, it doesn’t affect nodes PDH and DH, ND can recover through P14, NDHwill also recover through N2 and N3. Similar analysis can be derived if assuming nodes PDH and NDH store “0”, nodes PD,ND, and DH store “1”.

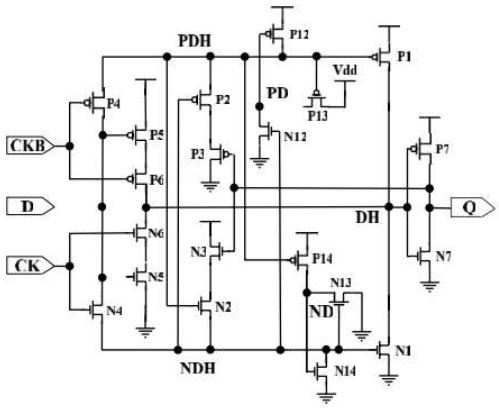

Fig. 5. Proposed master latch

PROPOSED SLAVE LATCHES:

Fig. 6 shows the proposed-I slave latch. Compared with the type-A latch, ten additional transistors (P10, P11, P12, P13, P14, N10, N11, N12, N13, and N14) are added to the proposed-I slave latch. The aim of adding transistors P12, P13, P14, N12, N13, and N14 has been discussed in section III, that is, guaranteeing nodes PDH and NDH are always connected to either GND or Vdd. Except for these six transistors, the only differences between the Proposed-I slave latch and type-A slave latch are that the positions of N11 and P10 are swapped, and the gates of thep10 and N11 are connected to output Q. This change can overcome the defect that N10 and N11 cannot charge DH in type-A slave latch, meanwhile, it solves the problem that DH takes a high-impedance state and leakage will happen when node PDH or NDH is hit.
In the system operation mode, CNF is 0, and P8, P9, N8, and N9 are on. When the clock is high, P4 and N4 are on, and the slave latch is in its transparent mode. The additional transistors P10 and P11 are on, but N10 and N11 are off. Assume input data is “0”, and then node DH is “1”, nodes PDH, NDH, and Q are “0”. Therefore, node DH is connected to Vdd through P1 rather than P10 and N10, in other words, N10 (P11) and P10 (N11) are not

turned on at the same time during normalsystem operation. When the clock is low, P4 and N4 are off, and the slave latch is in its hold mode. If a strike occurs on node PDH, DH will not take a high-impedance state due to the turn-on transistors N10 and P10, and with the help of the turn-on transistors P2 and P3, PDH is recovered to its original state. the Й1transition can only occur on PDH, and the Й0transition can only occur on NDH.

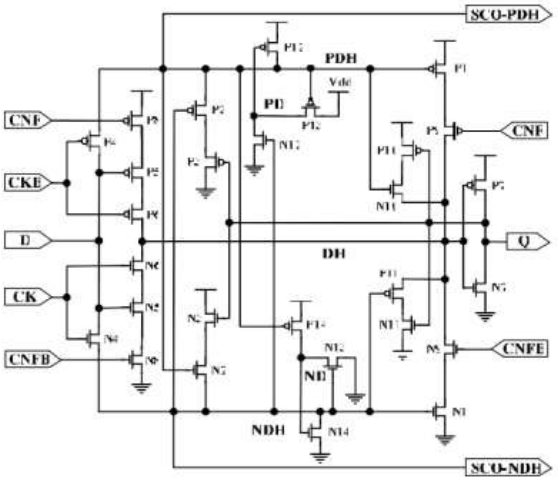

Fig. 6. Proposed-I slave latch

Fig. 7 shows the proposed-II slave latch. Compared with the proposed-I slave latch, the only difference is that either the drains of N10 and P11 are connected to the drains of P1 and N1 or to node DH. By connecting drains of P11 and N10 to thedrains of P1 and N1, the proposed-II slave latch overcomes the defect that the proposed-I slave latch introduces more delay at the Q output. Furthermore, the capacitance of node DH in the proposed-I slave latch is larger than that in the proposed-II slave latch, in other words, the critical charge of the proposed-I slave latch on node DH is larger than that of the proposed-II slave latch on the same node.

The proposed-I and proposed-II slave latches have the similar operation, here it needs not to repeat again. By analyzing, the conclusion can be easily get that the additional transistors in proposed-I and proposed-II slave latches do not affect the values stored in PDH, NDH and DH in scan-shift operation.

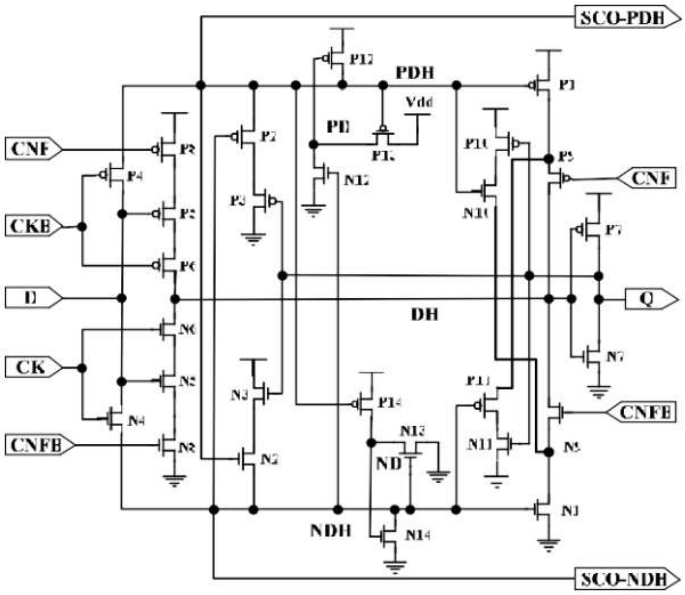

Fig. 7. Proposed-II slave latch

SIMULATION RESULTS:

In this section, the gate widths/lengths of PMOS and NMOS transistors are set to 1600nm/60nm and 600nm/60nm, respectively, except for P0, N0, P12, and N14. For the reason described in section III, P0 and P12 are set to 800nm/60nm, and N0 and N14 are set to 300nm/60nm. The exponential current source used in this paper can be expressed

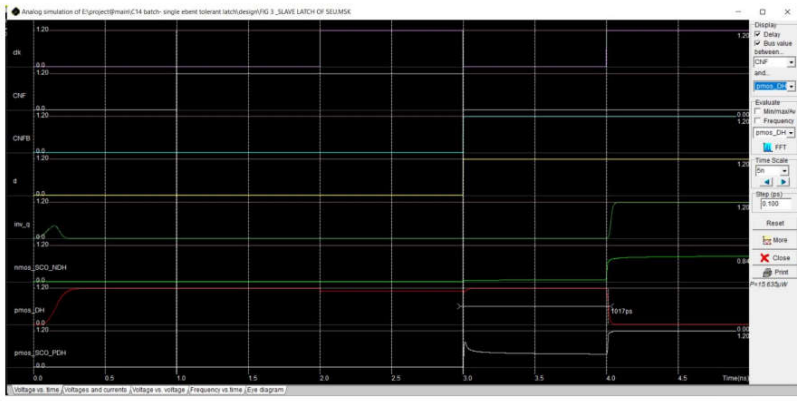

Fig. 8. Timing diagram of the proposed-I slave latch

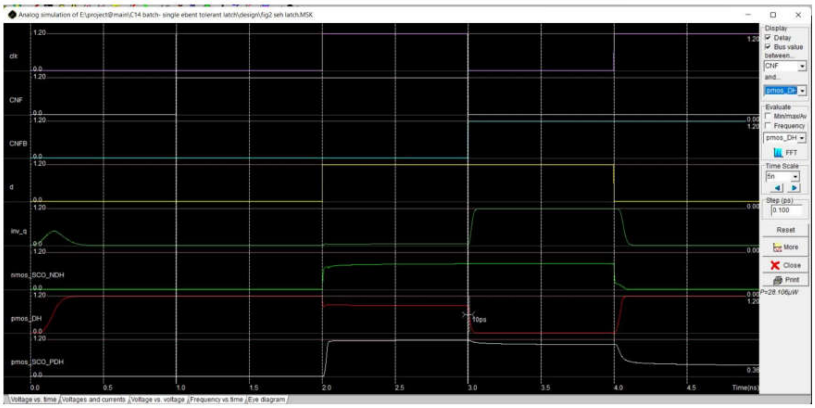

Fig. 9. Timing diagram of the proposed-II slave latch.

Figs. 8 and 9 show the SEU results due to a 1 pC disruption at each node. We can see that no errors appear at the output node.

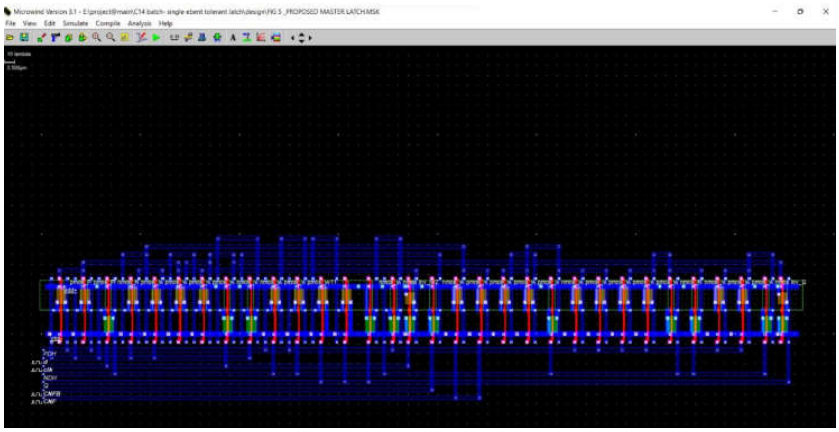

Fig. 10. Layout of a) proposed slave latch

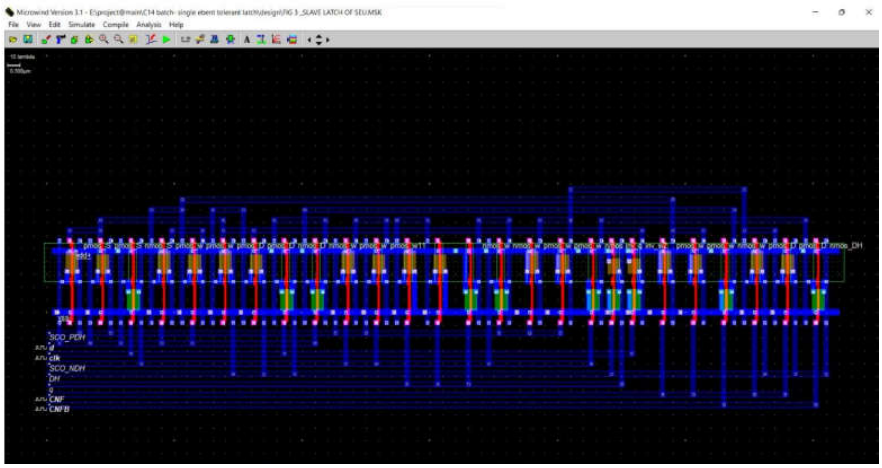

Fig.10. b) proposed master latch

Fig.10 are the layouts of proposed master latch and slave latches. We have also redrawn the layout of SEH latch, Type-A, Type-B, Type-I, and Type-II latches to make comparisons, and the results are shown in Tab. I. The proposed master latch has 140% area overhead of SEH, and our proposed slave latches have 159%, 139%, 130% area overhead of Type-I, Type-II, and Type-A, respectively. Besides, in terms of static power consumption, our proposed master latch and slave latches are much larger than the other latches, this is due to the increased number of transistors. However, these increasing transistors guarantee that all internal nodes are always connected to either Gnd or Vdd in hold mode, which effectively avoid data loss when the latch must hold for a long time.

TABLE- I; COMPARISONS

	Static Power (μW)	**T*p*CK-Q(ps)**	**Aera(μm^2)**
SEH	0.16	37.66	11.78
Type-I	0.19	59.82	13.57
Type-II	0.19	57.84	15.47
Type-A	0.26	85.91	16.59
Type-B	0.25	74.09	16.59
Proposed-I	1.50	96.29	21.59
Proposed-II	1.49	83.61	21.59
Proposed master latch	1.29	38.58	16.52

The CK-Q delay is measured as stated in [9]. Form Tab. I, we can see that, our proposed-I latch has the longest average CK-Q delay, which is 161%, 166%, 112%, 130% of Type-I, Type-II, Type-A, and Type-B respectively. Besides, our proposed master latch has almost the same CK-Q delay as that of SEH latch. Our proposed-II latch has a comparable CK-Q delay compared with Type-A and Type-B, but is a little higher than that of Type-I and Type-II. According to the above analysis, our proposed latch has the worst performance considering static power, area, and CK-Q delay. However, as discussed in section II, III, and IV, our proposed latches have effectively avoided data loss when held for much longest time, so the performance degradation is worthy.

CONCLUSION:

In this paper, two slave latch and a master latch are proposed for SEU tolerance and scan delay testing. The proposed slave latches can tolerate disruptions up to 1pC. Besides, a set of simulation results has been done,

which shows that the area and power consumptions are all increased compared with other state-of-the-art latches. However, considering our main purpose of this paper is to solve the problem of avoiding data loss, it is worthy.

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