DESIGN OF PROPOSED MAJORITY GATES IN QUANTUM DOT CELLULAR AUTOMATA DESIGNER

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ABSTRACT:

Quantum-dot cellular automata (QCA) are promising models in nanotechnology grounded on the single electron effects of quantum dots and molecules. QCADesigner software will be used to create a detailed layout and for circuit simulation. A Quantum-Dot Cellular Automata (QCA) has long been deemed to be an alternative or supplementary to complementary metal oxide semiconductor (CMOS) technology in theory in the future. In general, QCA works indispensably through a four-phase clocking mechanism.A majority gate is a logic gate that produces an output signal based on the majority of input signals. The gate has multiple input signals and a single output signal. A Static Random Access Memory (SRAM) and Look-Up-Table (LUT) is then built to achieve a significant reduction in hardware cost. The proposed circuits can correct functions and advantages in area, cell count, delay, cost, and energy dissipation compared with previous designs. These circuits are easy to be extended to 16-bit, 32-bit, or advanced bit. The proposed Majority gate design can achieve high-speed functionality while maintaining a low power consumption. The proposed design is scalable and can be implemented in larger QCA circuits. This design will provide an important building block for future QCA-based computing systems.

Keywords : Four-phase clocking mechanism, Static Random Access Memory, Look-Up Table, Quantum Dot Cellular Automata.

INTRODUCTION

QUANTUM-DOT cellular automata (QCA) decreases power consumption and delay. It further increases frequency and speed in the transmission of information. It has high operational speed (tera hertz range) , low-power consumption, high device density. It has homogenous structure which makes an easy nano scale fabrication. A 16-bit × 32-bit SRAM implemented in QCA with minimum delay in read (R) and write (W) operations uses the least possible area and hence it has lesser delay when compared to CMOS. So, with the 16bit X 32bit SRAM improves minimum area and complexity with minimum delay [5].Static random-access memory (static RAM or SRAM) is a type of arbitrary-access memory that uses latching circuitry (flip-flop) to store each bit. SRAM is volatile memory in which data is lost when power is removed. SRAM can be used to create a speed-sensitive cache. SRAM only has medium power consumption. SRAM has a shorter cycle time since it doesn't bear breaking between accesses. The size of CMOS has decreased but there are still some limitations and hence Static random access memory (SRAM) represents an attractive application of the QCA technology [6].QCA offers faster speed, lower size, and lower power consumption than transistor-grounded technology. QCA is based on the interaction of bi-stable QCA cells constructed from four quantum-dots.. Each cell is constructed from four quantum dots arranged in a square pattern. The cell is charged with two electrons, which are free to lair between conterminos dots. Electrostatic repulsion takes place mutually between electrons. The design and simulate the LUT-SR optimized RNG using CMOS is done. Proposed design using QCA in VHDL language with the help of Xilinx tool[7].There are two stable states in each cell and these stable states are equal to logics "0" and "1" in digital circuits. In digital circuits the most crucial element is memory and there are two kinds of memory i.e Content-Addressable Memory (CAM) and Random Access Memory (RAM). CAM is accessed in parallel and can be used in CPU of computers. CAM circuit consists of memory unit and an identity gate. The new memory unit was utilized to

develop CAM circuit in the QCA technology. The results are obtained using QCA Designer tool version 2.0.3[8].The main advantage of QCA technology is, it minimize the amount of energy dissipation. Two clocking schemes, namely Landauer clocking and Bennett clocking and are analysed for energy dissipation and performance analysis of QCA systems. The equality reserving nature of the Fredkin gate helps the proposed gate to be fault tolerant. Using these basic reversible gates we want to design the RAM and ALU for the future generation Quantum Computer [9].

QCA REVIEW

A QCA clock induces four stages in the tunneling walls of the cells above it. In the first stage, the tunneling walls start to rise. The alternate stage is reached when the tunneling walls are high enough to help electrons from tunneling. The third stage occurs when the high hedge starts to lower.

A typical QCA design requires four timepieces, each of which is cyclically 90 degrees out of phase with the prior clock. If a horizontal wire consisted of say, 8 cells and each successive pair, starting from the left were to be connected to each successive timepiece, data would naturally flow from left to right.

The first brace of cells will stay latched until the alternate brace of cells gets latched and so forth. In this way, data inflow direction is controllable through timepiece zones. There is a connection between quantum-dot cells and cellular automata. Cells can only be in one of 2 states and the tentative change of state in a cell is mandated by the state of its conterminous neighbours. However, a system to control data inflow is necessary to define the direction in which state transition occurs in QCA cells. The timekeepers of a QCA system serve two purposes powering the automaton, and controlling data flow direction. QCA timekeepers are areas of conductive material under the automaton's chasis, modulating the electron tunneling walls in the QCA cells above it.

Quantum dots are bitsy nanocrystals that glow when stimulated by an external source similar as ultraviolet (UV) light. How numerous titles are included in the quantum dot determines their size and the size of the quantum dot determines the colour of light emitted.

The clocking of QCA can be fulfilled by controlling the potential walls between conterminous quantum-dots. The timepiece used in QCA consists of four phases: hold, release, relax, switch. It's considered that the pause between conterminous phases is 90°.

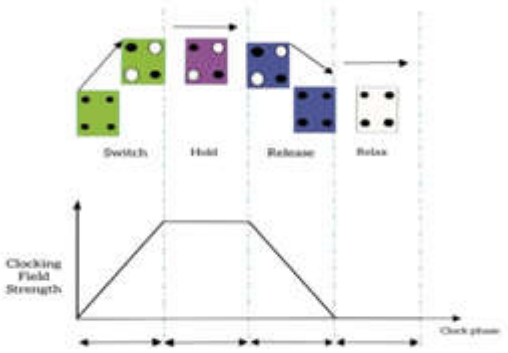

Fig.1: Clocking Mechanism in QCA

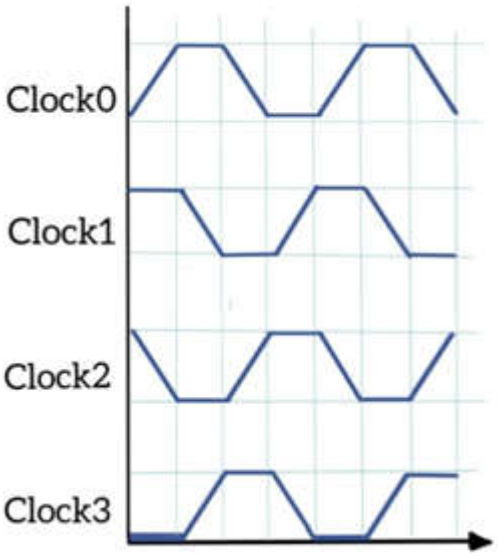

Fig. 2: QCA clock zones

RELATED WORKS:

Three input majority gates

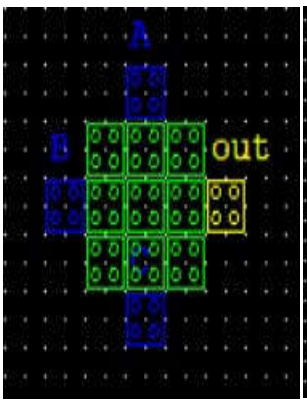

Fig. a

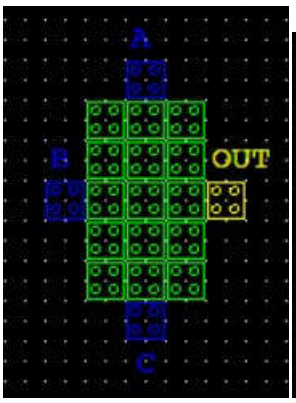

Fig. b

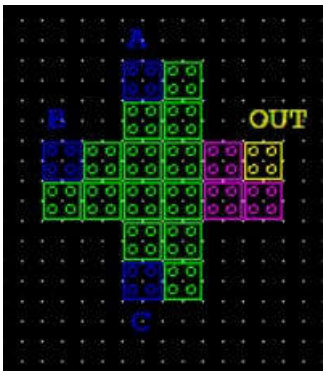

Fig. c

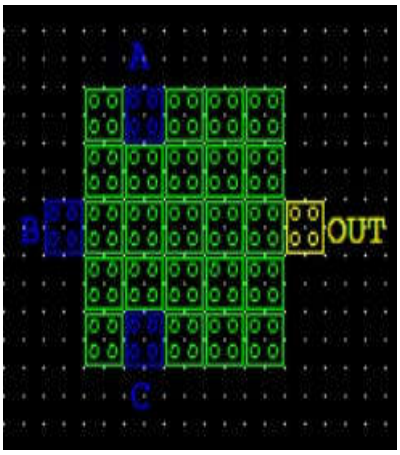

Fig. d

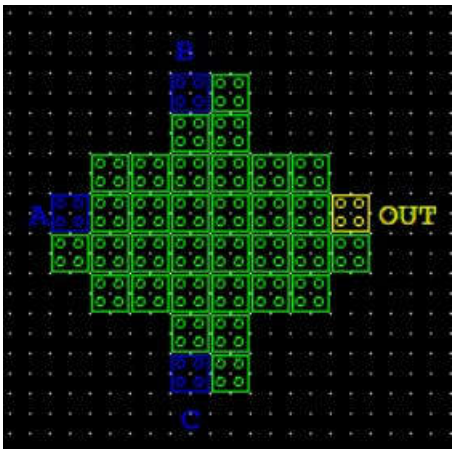

Fig. e

3.2 Five input majority gates

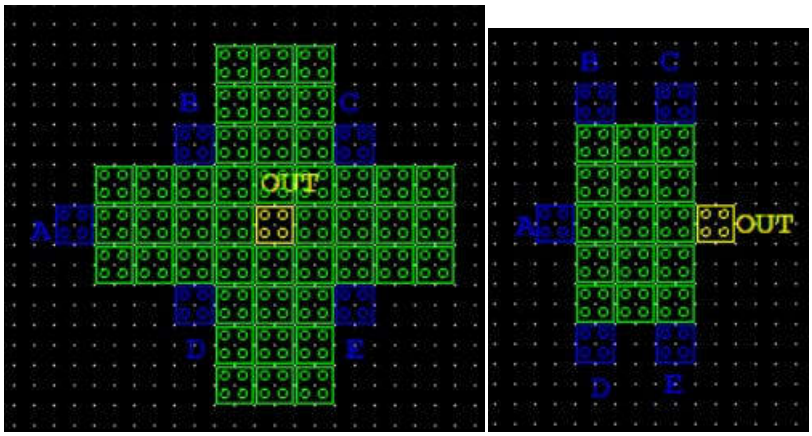

Fig. a Fig. b

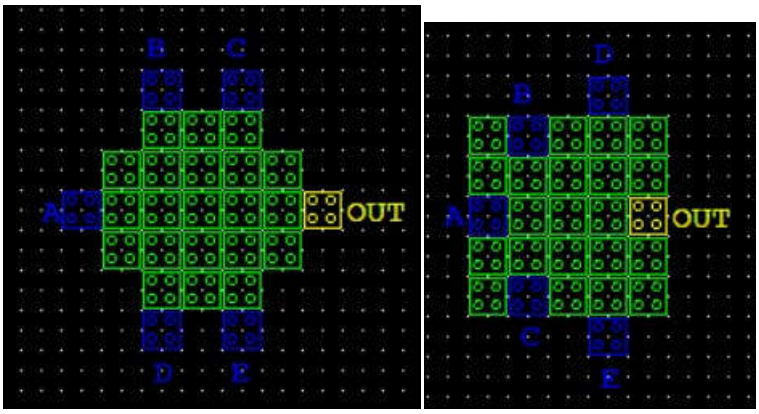

Fig. c Fig. d

Das and De [10] proposed a three-input majority gate with 13 cells and occupied area of 0.01 μm2 , and energy dissipation of 3.47e-4eV.

Du et al. [11] introduced a fault-tolerant three-input majority gate with 19 cells and occupied area of 0.03 μm2 and energy dissipation of 5.20e-4eV.

Kumar and Mitra [12] proposed a three-input majority gate with 20 cells and occupied area of 0.02 μm2 , and energy dissipation of 1.83e-3eV.

Sen et al. [13] suggested a three-input majority gate with 27 cells and occupied area of 0.03 μm2 , and energy dissipation of 1.45e-3eV.

Wang et al. [14] proposed a three-input majority gate with 36 cells and occupied area of 0.04 μm2, and energy dissipation of 2.16e-3eV.Although it has a good tolerance, it has a high complexity.

Farazkish [15] designed a five-input majority gate with 50 cells and occupied area of 0.04μm2 and and energy dissipation of 1.85e-3eV..One of the drawbacks of this gate was that the output was located in the middle and required a multilayer structure to design the circuit.

Du et al. [16] proposed a five-input majority gate with 22 cells and occupied area of 0.03 μm2, and energy dissipation of 6.40e-4eV.

Goswamiet al. [17] presented a five-input majority gate with 27 cells and occupied area of 0.03 µm2 and energy dissipation of 8.20e-4eV.

Sun et al. [18] proposed a five-input majority gate with 27 cells and occupied area of 0.03 µm2 , and energy dissipation of 2.24e-3eV.

PROPOSED DESIGNS:

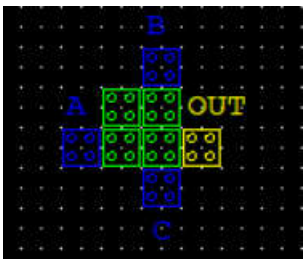

Fig. 4.1: Proposed 3-input majority gate

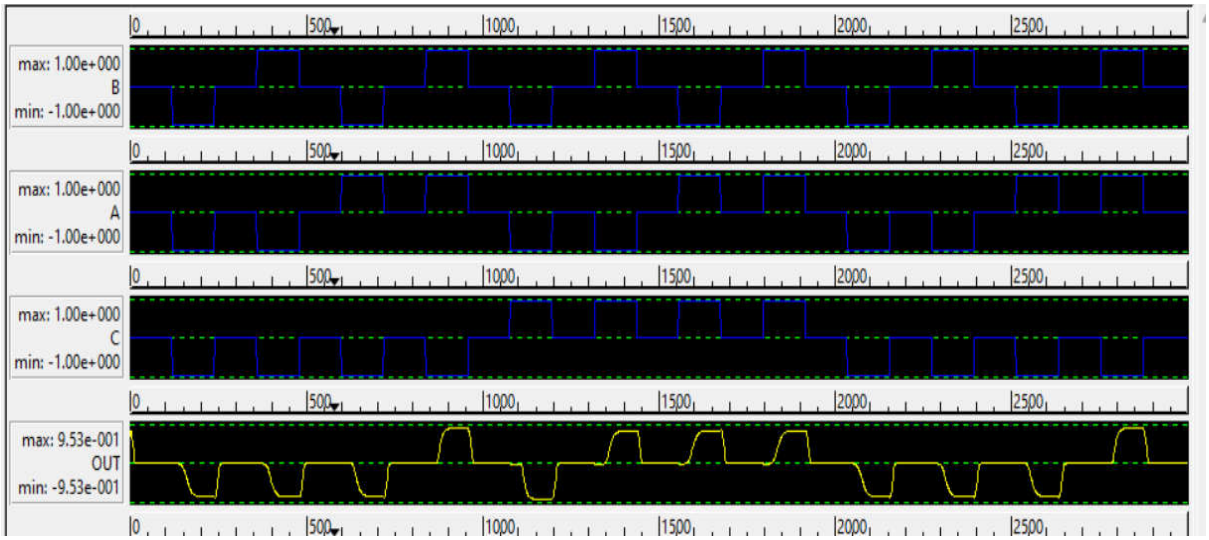

Fig. 4.2: Proposed 3-input majority gate simulation result

Proposed Three Input Majority Gate:

For this proposed digital logic gate, three digital inputs are considered based on the given inputs, the decision cells will make a decision which gets carried on to the output.

If any two of the given inputs are high, then decision cells will automatically set to high based on the decision cells the output will set to high

If in case any two of the given inputs are low, , then decision cells will automatically set to low based on the decision cells the output will set to low

Here it can be stated that, a majority gate returns true if and only if more than 50% of its inputs are true.

So, it can be end up with the same configuration based on the given inputs that gets carried on to the output.

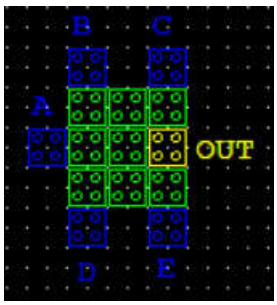

Fig. 4.3: Proposed 5-input majority gate

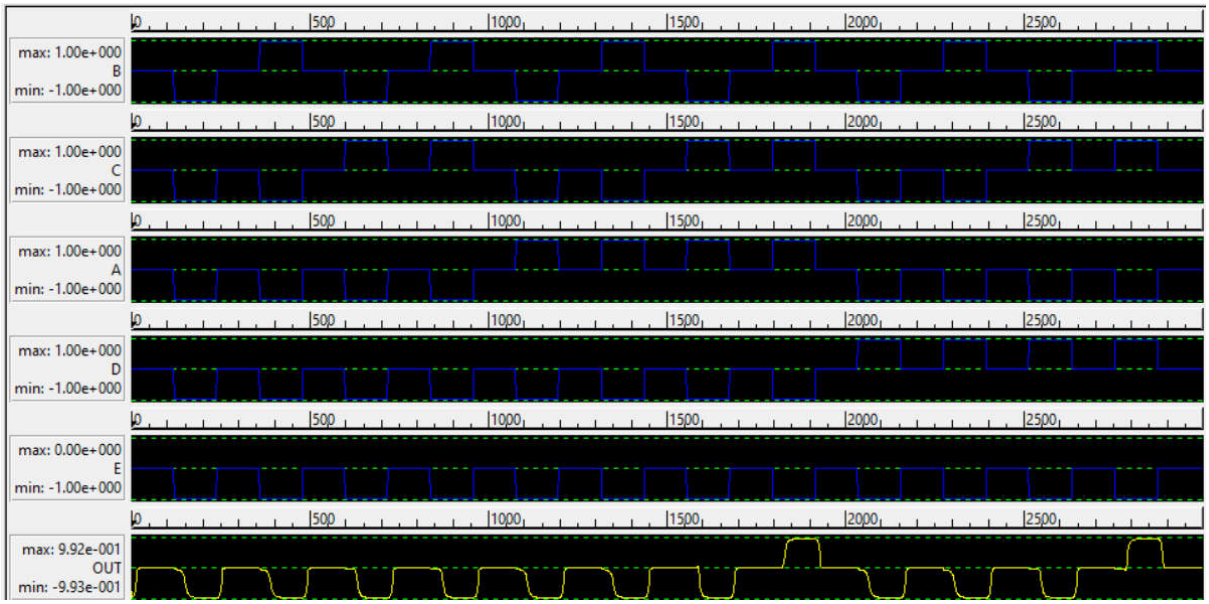

Fig. 4.4: Proposed 5-input majority gate simulation result

Proposed Five Input Majority Gate:

For this proposed digital logic gate, Five digital inputs are considered based on the given inputs, the decision cells will make a decision which gets carried on to the output.

If any three or more of the given inputs are high, then decision cells will automatically set to high based on the decision cells the output will set to high.

If in case any three or more of the given inputs are low, , then decision cells will automatically set to low based on the decision cells the output will set to low.

Here it can be stated that, a majority gate returns true if and only if more than 50% of its inputs are true.

So ,it can be end up with the same configuration based on the given inputs that gets carried on to the output.

RESULTS AND CONLUSION:

Table.5.1: Proposed 3-input majority gate comparison

3-input Majority gates	Energy (eV)	Count(no. of cells)	Area(μm^2)
a[10]	3.47e-4	09	0.01
b[11]	5.20e-4	15	0.03
c[12]	1.83e-3	13	0.02
d[13]	1.45e-3	23	0.03
e[14]	2.16e-3	32	0.04
Proposed 3-input gate	2.65e-4	04	0.01

Table.5.2: Proposed 5-input majority gate comparison

5 input Majority gates	Energy (eV)	Count(no. of cells)	Area(μm^2)
a[15]	1.85e-3	44	0.04
b[16]	6.40e-4	15	0.03
c[17]	8.20e-4	21	0.03
d[18]	2.24e-3	21	0.03
Proposed 5-input gate	4.84e-4	08	0.02

CONCLUSION:

When comparing the existing majority gates with the proposed majority gate , it can be concluded that area ,cell count, and energy dissipation of the proposed majority gate has reduced to less values. By using this proposed majority gate, SRAM and an LUT is then built to achieve a efficient results in energy consumption, area and cell count. With these, it allows further integration of other components which can reduce overall size of the device, cost of manufacturing and enhances the yield of the chip. So, it makes SRAM a popular choice for modern electronic devices that requires high performance.

SRAM	Energy (eV)	Count(no. of cells)	Area(μm^2)
4 bit SRAM	4.09e-3	145	0.21
Proposed 4bit SRAM	3.80e-3	141	0.20

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