DESIGN OF PROPOSED LOW POWER 4-BIT ALU DESIGN USING FS-GDI APPROACH WITH 45 NM TECHNOLOGY

Dr J Sudhakar[1], **S Usha Sri**[2], **S Divya Chandana**[3], **B Priyanka**[4], **U Meghana**[5]and **V Sri Hasika**[6]
[1] Professor & Principal, Vignan's Institute of Engineering for Women, Duvvada.
[2,3,4,5,6] UG Students, Dept. of ECE, Vignan's Institute of Engineering for Women, Duvvada.
[2]Ushasri.setti@gmail.com

ABSTRACT

In electronics, the arithmetic and logic unit(ALU) is the main component in the data processing such as encoding and decoding in the communication systems. The power consumption is related directly to the computational complexity of the system due to the data protection schemes and amount of transmitted data. The ALU is the core component of the data/image processing and DSP. Therefore, improving the characteristics of ALU directly improves the efficiency of data/image processing. This paper proposesa design for the Arithmetic Logic Unit (ALU) utilising the FS-GDI approach to overcome the drawbacks in the terms of power consumption, circuit complexity and propagation delay. The presented ALU is designed in 45 nm node technology using Mentor Graphics. These ALU unit can also be extended to 16-bit, 32-bit, or higher bit.

KEYWORDS- Arithmetic and Logic Unit, Full Swing Gate Diffusion Input (FS-GDI), Digital Signal Processing (DSP)

INTRODUCTION

An application of wireless/mobile technologies covers various fields such as military, civil, environmental monitoring and healthcare. These technologies face many constraints in the applications spreading like the energy resources constraints. The amount of required/ consumed power for operating these devices is became one of the fundamental limits in portable systems . The power consumption is related directly to the computational complexity of the system.

The arithmetic and logic unit is the main component in the data processing such as the data encoding and decoding in the communications systems. This paper presents various ALU designs for improving the power efficiency of mobile devices and data processing circuits. The increasing demand for low power VLSI achieved at different design levels, such as the architectural, circuit and the process technology level. At the circuit design level, considerable power savings exists by means of proper choice of a logic style for implementing combinational circuits .

The logic style is used in realising the digital circuits basically influences the speed, size (no. of transistors), power dissipation and the wiring complexity of the realized circuits . Improving the power and speed efficiency of the digital circuits or communications systems can be performed by efficient hardware design and choosing suitable logic style for realising these circuits. There are several techniques can be employed for enhancing the power efficiency of the data/image communications systems, the image processing and transmission over mobile communications channel with considering the low power system is presented. Utilising the power efficient logic style approach for realising the logic and digital circuits is suitable for providing sufficient performance enhancement. The FS-GDI is used for realising the FA, logic functions and ALUs to implement power efficient units in this paper. The power limits the error control codes and security techniques utilising in lowpower wireless networks such as the WSNs and Wireless Personal Area Networks (WPANs).

LITERATURE SURVEY

During the last few years, the development of low power circuits have been studied, and various metrics have been determined to measure the performance of ALU design ,

Mehedi et al., 2020 proposed the Delay Time Metric(T) where speed efficiency of the proposed ALUs unit is evaluated using this metric.[1]

Kishore & Ramachandran, 2019, The amount of the consumed power is considered as a performance metric. The proposed ALUs design achieves 30.0% improvement in the amount of consumed power compared to the previous ALUs design.[2]

Chua-Chin et al., 2020, Cadence tools package is used for designing the proposed hybrid Full Adder (FA) circuit, It is proposed to improve the delay time and reduce the computation. The combination between the pass transistors (PTs), transmission gates (TGs) and the traditional CMOS approaches are employed in the proposed hybrid technique for implementing the proposed FA circuit. The performance of the proposed hybrid FA is evaluated using the speed and power delay product metrics.[3]

Nagalakshmi & Kavya ,2018 presented 32-bit Carry Increment Adder (CIA) circuit using the slice approach and implemented by the Pass Transistor Logic (PTL) technique.The proposed CIA circuit acts better than the previous circuits due to the improved power consumption, delay time and throughput performance parameters. and testing are executed by the BSIM4 simulation package.[4]

In Bhagyalaxmi et al. (2015), 10 T FA circuit has been used for building 16-bit ALU unit in 180 nm CMOS process. This power efficient FA is utilised for improving the whole power efficiency of ALU unit.[5] PTL logic style is used to design and implement 8 T FA circuit **[6]**(Bhattacharyya et al., 2015). This FA improved the consumed power by 70% compared to TG-based design. The various technology nodes are considered for improving the ALU performance **[7]** (Kumar & Sharma, 2017).

LOW POWER DESIGN APPROACHES

Different technologies of low power of VLSI design are presented. The various traditional logic styles have some advantages and disadvantages, such as, the CMOS logic style is popular and widely used approach, it is low power. On the other hand, it suffers some disadvantages such as, high power consumption, inefficient area approach. Choosing suitable logic style for realising the required logic and digital circuits improves their performance, there are several traditional logic styles such as, PTL, TG, CPL and DPL, it is presented as modified-CPL approach.

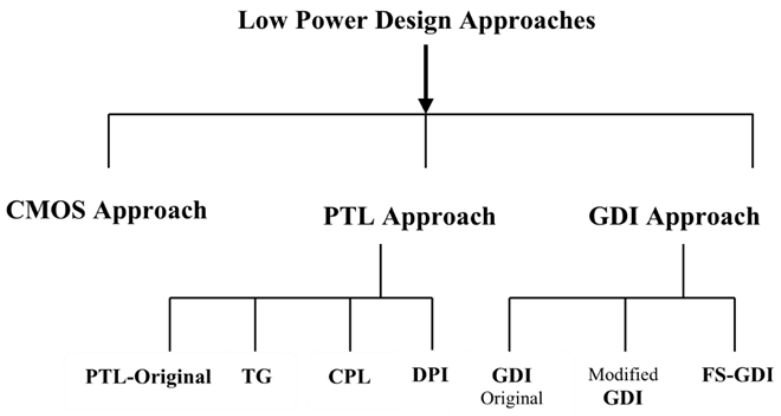

Fig 1: Low Power Design Approaches

GDI TECHNIQUE

Gate Diffusion Input (GDI) technique is a digital circuit design technique used to reduce power consumption and area in integrated circuits. It achieves this by using a combination of p-type and n-type MOSFETs to implement logic functions. In traditional CMOS circuits, a single n-type or p-type transistor is used to implement a logic function. However, in GDI, two transistors are used to implement a logic function: a p-type transistor connected to the gate of an n-type transistor. The p-type transistor acts as a "diffusion barrier" and controls the input signal to the n-type transistor.

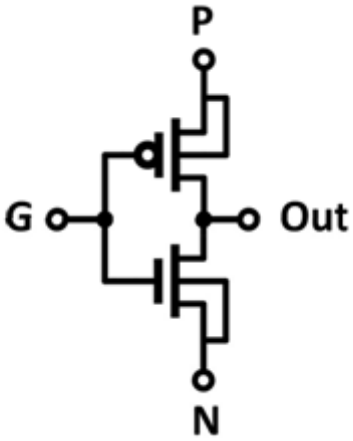

Fig 2:GDI Cell

MODIFIED GDI TECHNIQUE

The Modified Gate Diffusion Input (MGDI) technique is an improvement over the traditional GDI technique that addresses some of its limitations. The primary goal of MGDI is to reduce the delay and increase the noise immunity of GDI circuits. In MGDI, an additional transistor is added to the GDI cell to improve the noise immunity. This additional transistor is connected in parallel with the n-type transistor and acts as a noise filter. The noise filter is used to suppress the noise that could otherwise affect the input signals.

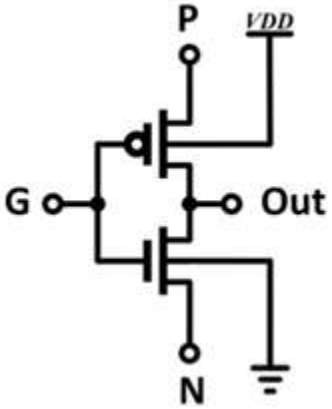

Fig 3: Modified GDI Cell

FULL SWING GATE DIFFUSION INPUT (FS-GDI) TECHNIQUE

Full- swing GDI cells proposed to enhance the output swing of GDI gates as an preference for swing restoration buffers, a swing restoration transistor used to enhance the output swing of F1 and F2 gates. It is a type of input buffer circuit that is used to amplify and buffer a small input signal to a larger voltage level that can be used by the subsequent stages of the circuit.

In the full swing gate diffusion input, the input signal is applied to the gate of a MOSFET transistor, which is connected in parallel with another MOSFET transistor that is used for biasing. The gate of the biasing transistor is connected to the power supply voltage, while the gate of the input transistor is connected to the input signal. When the input signal is low, the input transistor is turned off and the biasing transistor is turned on, pulling the output voltage to the power supply voltage. When the input signal is high, the input transistor turns on and starts pulling the output voltage towards the ground voltage. The output voltage swings between the power supply voltage and the ground voltage, providing a full voltage swing.F1 and F2 are universal gates analogous to NAND and NOR gates as shown inFig1 Using this approach full swing output can be achieved at the expense of escalating transistor count compared to modified- GDI gates, but when compared to CMOS and PTL performances FS gates uses smaller transistors hence power consumption and area of VLSI circuits are reduced.

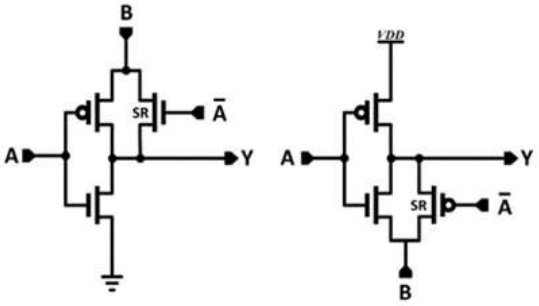

Fig 4: FS-GDI Cell

RELATED ALU DESIGNS:

The 1-bit ALU is presented in Figure 2.

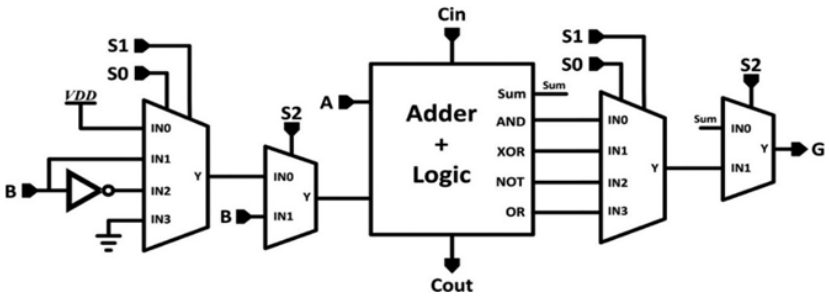

Fig 5: Schematic of 1-bit existing ALU

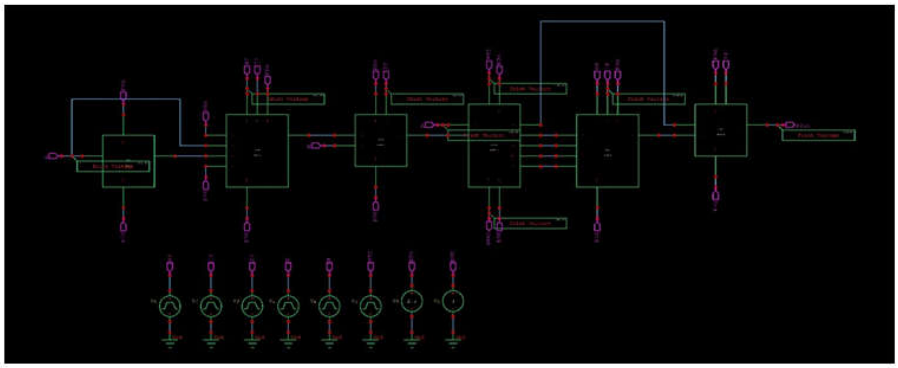

Fig 6: Schematic of 1-bit ALU stage

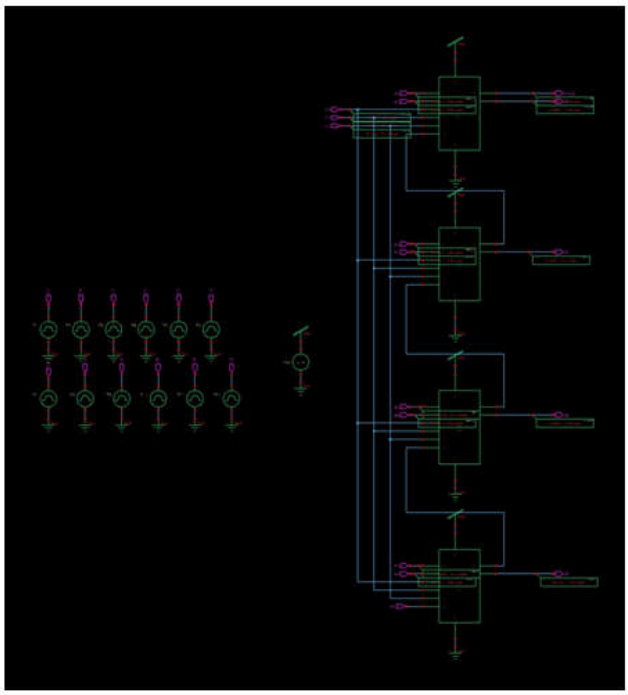

Fig 7: 4-bit ALU constructed by 1-bit unit

PROPOSED METHODOLOGY

The second proposed design of the ALU based on the FS-GDI approach is presented. This design aims to decrease the delay time and optimises the speed efficiency of the 4-bit ALU. The delay time (D) is optimised with maintaining low-power operation and full-swing output. The low-power FA is employed in this ALU design, it is realised using FS-GDI logic style, it consists of 18 transistors as given in Figure 8. The 1-bit ALU as shown in Figure 8, it contains {FA, logic block, (2x1) multiplexer, two (4x1) multiplexers, and an inverter}. The proposed 4-bit ALU is shown in fig 8.

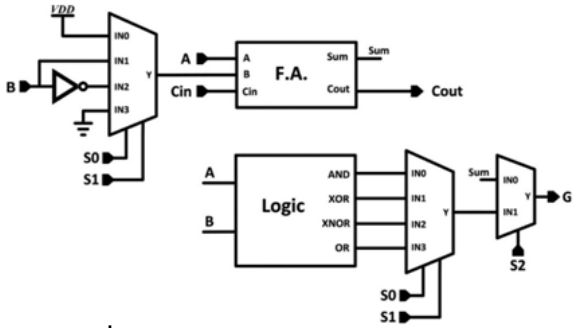

Fig 8: Block Diagram of Proposed ALU

RESULTS AND DISCUSSIONS

The proposed 1-bit ALU design is shown in fig 9.

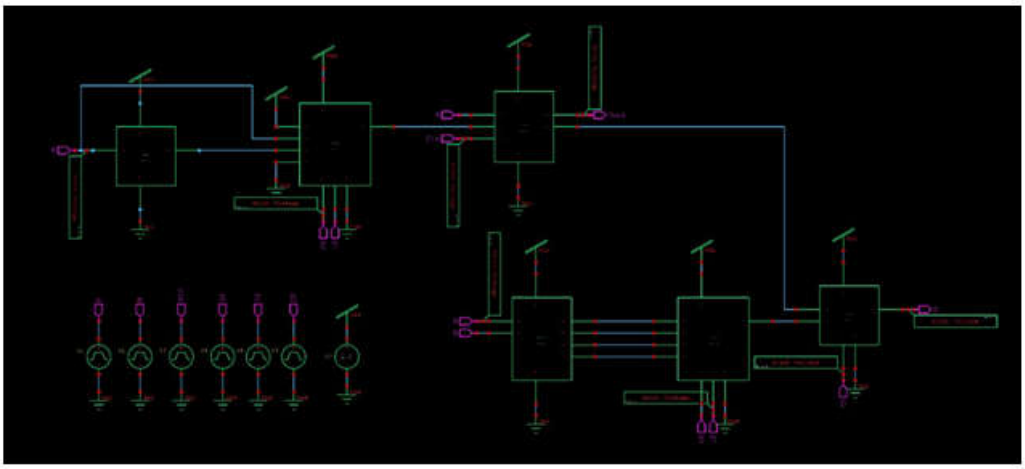

Fig 9: 1-Bit ALU

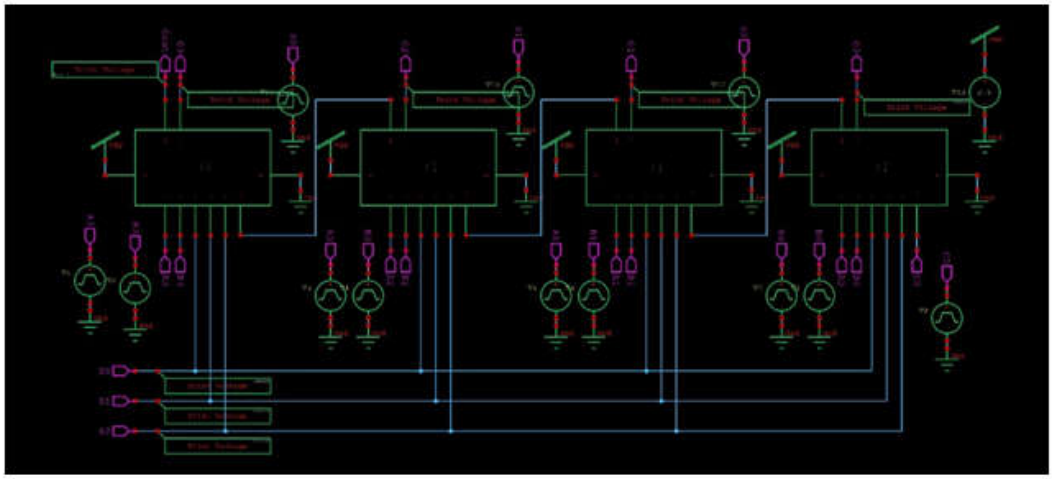

Fig 10: 4-Bit ALU

The 4-bit ALU design using 1-bit ALU is shown in fig 10.

RESULTS AND DISCUSSIONS:

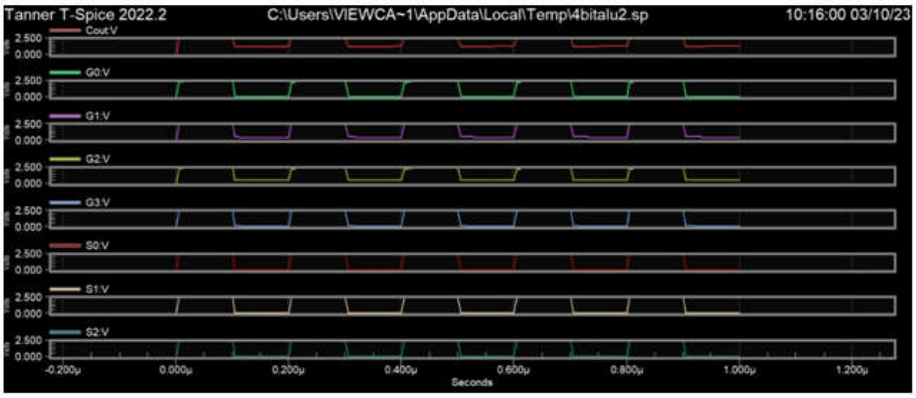

Fig 11: Output Waveform of 4-bit ALU

Metric Comparison of the ALU units:

ALU Units	**Power(µW)**	**Delay(ps)**	**Transistor Count**	**PDP(e-18J)**
Existing unit	27.110	36.86	286	999.275
Proposed unit	15.36	19.05	294	292.608

The circuit of the proposed ALU unit is implemented in 45nm node technology. From results of proposed ALU. It achieves speed efficient by decreasing the delay-time by 22.31% and improves energy efficiency by 21.2%. Delay time of ALU is optimised compared to existing ALU.

CONCLUSION

This paper aims to improve performance of ALU units and presents power efficient 4- bit unit. It studied behavior of a FS-GDI-based ALU in 45 nm technology using Mentor Graphics. In the proposed design , delay time is reduced by 22.31% compared to the existing ALU, (PDP) of ALUII reduced by 21.21% compared to existing ALU. Proposed ALU design consists of 294 transistors; both designs operate under Vdd = 2.5 V. The proposed 4-bit ALU design are suitable for low energy high-speed VLSI applications. For Future scope, it can be extended to 8-bit, 16-bit, 32-bit and so on.

REFERENCES

[1] Mehedi, H., Jobayer, H., Mainul, H., Hasan, U. Z., & Sharnali, I. (2020), “design of a scalable low-power 1-bit hybrid full adder for fast computation,” circuits and systems II: express briefs, IEEE Transactions on August 2020, https://doi.org/10.1109/TCSII.2019.2940558 .

[2] Kishore, S., & Ramachandran, S. (2019). Ultra-low-voltage GDI-based hybrid full adder design for area and energy-efficient computing systems. IET Circuits, Devices & Systems, 13(4), 465–470. https://doi.org/10.1049/iet-cds.2018.5559

[3] Chua-Chin, W., Nanang, S., Tsung-Yi, T., & Yu-Hsuan, C. (2020). Multifunctional in-memory computation architecture using single-ended disturb-free 6T SRAM Zakaria, Zahriladha, Ahmed, Rabiah.

Advances in electronics engineering, lecture notes in electrical engineering (Vol. 619, pp. 49–57). Springer Nature Singapore Pte Ltd. https://doi.org/10.1007/978-981-15-1289-6_5

[4] Nagalakshmi, E. V., & Kavya, K. 2018. Design of 4 bit alu Using modified Gdi technology for power reduction. International Journal of Engineering Science Invention (IJESI).7:2. 38–45. Feb. 2018

[5] Bhagyalaxmi, T., Rajendar, S., & Srinivas, S. (2015). Power-aware alternative adder cell structure using swing restored complementary pass transistor logic at 45nm technology. Procedia Materials Science, 10(Cnt), 789–792. https://doi.org/10.1016/j.mspro.2015.06.021

[6] Bhattacharyya, P., Kundu, B., Ghosh, S., Kumar, V., & Dandapat, A. (2015). Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit. IEEE Transactions on Very Large Scale integration (VLSI) Systems, 23(10), 2001–2008. https://doi.org/10.1109/TVLSI.2014.2357057

[7] Kumar, P., & Sharma, R. K. (2017). An energy efficient logic approach to implement CMOS full adder. Journal of Circuits, systems and Computers, 26(5), 1750084. https://doi.org/10.1142/S0218126617500840

[8] Mukhedkar, M., & Pandurang, W. B. (2017). " A 180 nm efficient low power and optimized area ALU design using gate diffusion input technique," 2017 Int. Conference on Data Management, Analytics and Innovation ICDMAI, 47–51. doi:10.1109/ICDMAI.2017.8073484 2017

[9] Omnia, A., Mohsen, A., El-Bendary, M., Fathy, Z. A., & Said, M. S. (2019), "Design of area efficient and low power 4-bit multiplier based on full-swing gdi technique", 2019 IEEE International Conference on Innovative Trends in Computer Engineering (ITCE), Feb, PP. 328–333

[10] Shukla, R. L., & Mehra, R. (2014). Design analysis and simulation of 1 bit arithmetic logic unit on different foundaries. International Journal of Engineering Science, 2, 1–11. https://its.edu.in/RACE2016/RACE2015/RACE2014/finalpdfpapers/RACE1023.pdf