DESIGN OF MODIFIED BOOTH MULTIPLIER USING REVERSIBLE LOGIC GATES

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ABSTRACT

Reversible Multiplier is a computing device used to multiply two binary numbers by use of reversible address The design of a reversible multiplier is very important due to its wide range of applications in implementing computing systems using new technologies. In most multi-pliers presented so far, partial product generators and adders are designed separately.This increases the number of blocks that make up the final circuit. Reversible circuits have to use ancilla inputs and garbage outputs. The more blocks in a circuit, the greater the number of inputs and outputs. In this study, a column-wise structure is designed for the multiplier to reduce the number of individual blocks making it up. Increasing the size of reversible circuits in most new technologies is very costly. The number of blocks of the structure presented in this paper for a reversible multiplier is significantly reduced compared to existing designs. Moreover, the number of ancilla inputs and garbage outputs in each of these blocks is minimized. Therefore, the values of the secriteria in the proposed multiplie rare much lower than those of the previous works. In the proposed method, instead of designing the multiplier in two separate steps, each multiplier column is designed in the form of a block. Therefore, the number of blocks that makeup the circuit is equal to the number of the columns of the multiplication operation.

KEYWORDS : Reversible logic, Multiplier circuit, Quantum Cost, Garbage Outputs, Ancilla Inputs.

INTRODUCTION

The realization of booth's multiplier in reversible mode is considered as one of the fastest multipliers in literature. The field of Reversible Multiplier is a computing device used to Multiply two Binary Numbers by the use of Reversible Address. In reversible processing circuits there are computational components such as adders and multipliers.

Booth Algorithm

The algorithm was invented by Andrew Donald Booth in 1950 while doing research on crystallography at Birkbeck College in Bloomsbury, London. Booth's algorithm is of interest in the study of computer architecture. Andrew Donald Booth proposed Booth's multiplication algorithm which can perform the multiplication operation of Two Signed Binary numbers in their respective 2's complement form. A.D. Booth's encoding technique is also called as radix-2 booth's encoding algorithm.

Reversible Logic Gates:

Reversible Logic gates with a property of equal number of inputs and outputs, N-inputs and N-

outputs. When the number inputs and outputs are equal it will minimize energy loss during computations. The Reversible logic is designed, main purposed are decreased quantum cost, depth of the circuits and number of garbage outputs. The input and output vectors are mapped one-to-one in reversible gates, which have an equal number of outputs and inputs. The most basic reversible gates are 1x1 NOT and BUFFER. The Feynman, Toffoli, Peres and Fredkin gates are the widely used reversible logic gates.[1][10]

The number of Reversible gates(N): The number of reversible gates used in circuit.
The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. one cannot avoid the garbage outputs as these are very essential to achieve reversibility.

LITERATURE REVIEW

In this survey Multipliers are important components in computing systems, as they are involved in many processing operations. One of the common methods in implementing reversible multipliers is to divide them into two parts partial product generation circuit and summation circuit to add partial products and produce the final product. The preceding multipliers are contempted in this section Reversible logic is one of the most widely used topics in modern computing technologies, such as quantum computing, optical computing, and QCA[1]. Inreversible processing circuits, there are computational components, such as adders and multipliers. Many reversible system designers seek to design a reversible multiplier at a lower cost. The cost criteria include a variety of items, such as quantum cost, number of gates, number of ancilla inputs, and number of garbage outputs[2].
Since all components in a reversible system must be reversible, various components of such a processing system are implemented using reversible technologies [3]. Some of these components include various modules of the processor, such as registers, units of calculation and logic, memory, multiplexers, and so on. One of the most important parts of processing systems is the arithmetic and logic unit, which is responsible for performing various operations on the data. In many previous works carried out in this field, attempt shave been made to design various computational circuits, such as adders, multipliers, and arithmetic and logic units, with the reversible property and to reduce the value of different cost criteria as much as possible [9]. One of the interesting issues in this area is the design of the reversible multiplier. Multipliers are widely used circuits in processing systems, and making them reversible will often lead to increased costs. As noted earlier, the cost criterion can involve quantum cost, the number of gates, delays, or the circuit size interms of the number of inputs and outputs. reduced, the area is also reduced.

METHODOLOGY

PROPOSED MULTIPLIER STRUCTURE

The multiplication operation on two 4-bit values. The first two rows show the carry bits that we readed to each column and generated in previous columns. C_{ij} is the symbol of the carry bit generated in column I and added to column j. The third and four throws show two 4-bit numbers that are multiplied by each other. The a_i and b_j denote the i-th digit of A and the j-th digit of

B,respectively. The next four rows show the partial products denoted by a_ib_j . For simplicity, each of them is shown with P_{ij} here after. The final line shows the final product whose i-th digit is denoted by S_i.

A sex plained earlier,this multiplier consists of several sub-circuits. In each

Sub-circuit, only the operation is performed that is related to one of the columns of the multiplication operation. To clarify the issue, the following explain show to implement each column of multiplier separately.

IMPLEMENTATION OF COLUMN WISE MULTIPLIER

The only partial product calculated in column 0 is $P_{00}= a_0.b_0$. Therefore, only inputs a_0 and b_0 are needed to produce the output of column number 0, whose output is S_0.This column has no output carry bit

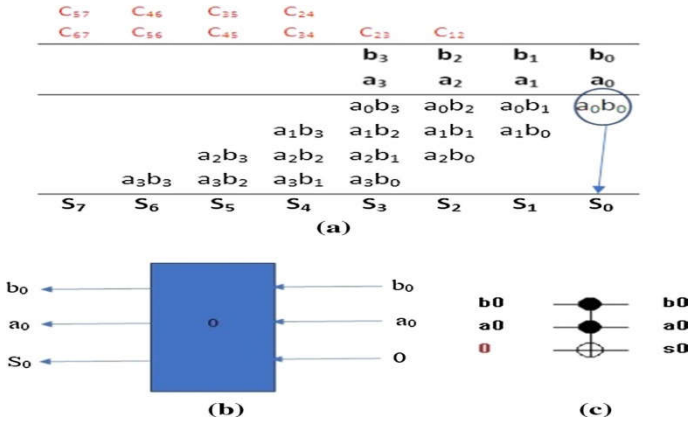

Fig.4 Block Diagram of Reversible Circuit of Column 0

The action performed in column1. In this column, a carry bit is generated, as well as one bit of the final product. Therefore, the output of this column is a two-bit value obtained from the sum of two partial products, $P_{01}= a_0.b_1$ and $P_{10}= a_1.b_0$.

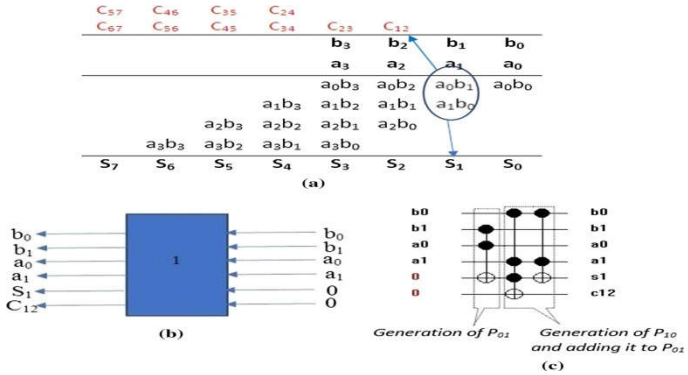

Fig.5 Block Diagram of Reversible Circuit of Column 1

It should be noted that C_{12} is the input carry signal to column 2, which takes the value S_2 at the output. However, C_{23} and C_{24} are constant inputs with a value of 0, which turn into the carry bits that are propagated to the next columns as the outputs. Briefly, this figure shows only some of the possible combinations for the three partial products P_{02}, P_{11}, and P_{20} and the input carry bit C_{12}.

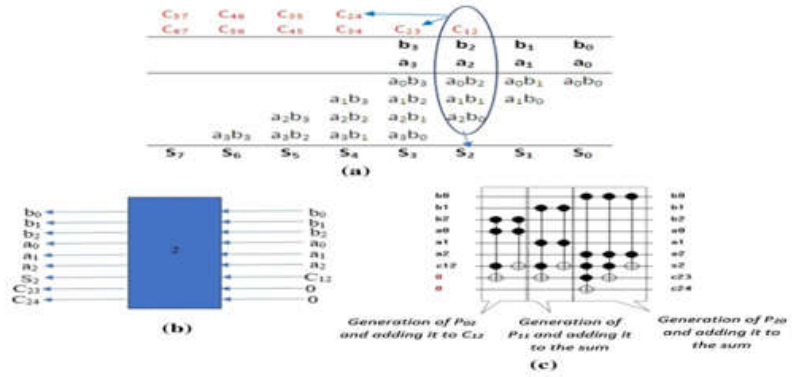

Fig.6 Block Diagram of Reversible Circuit of Column 2

This the column wise operation for column 3 and block diagram and reversible circuit generated for column 3 multiplier.

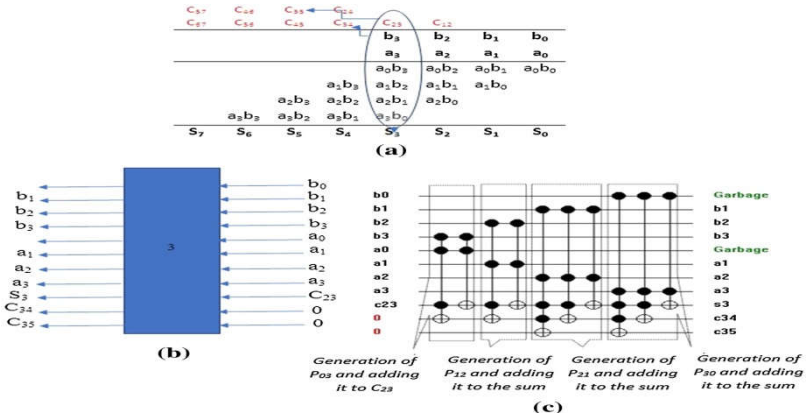

Fig. 7 Block Diagram of Reversible Circuit of Column 3

This the column wise operation for column 4 and block diagram and reversible circuit generated for column 4 multiplier.

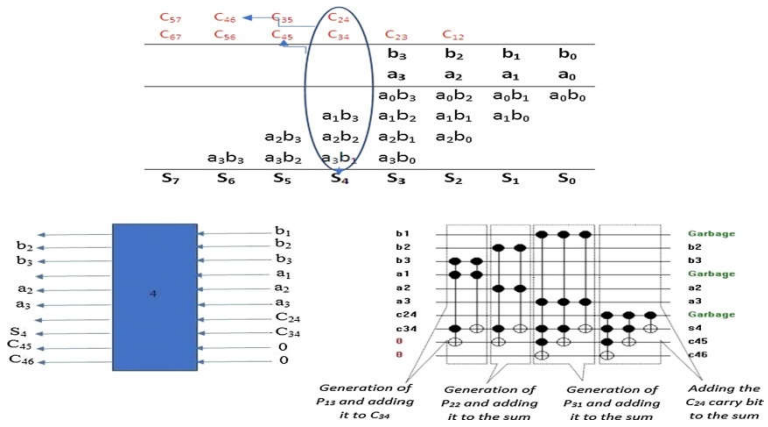

Fig. 8 Block Diagram of Reversible Circuit of Column 4

This the column wise operation for column 5 and block diagram and reversible circuit generated for column 5 multiplier.

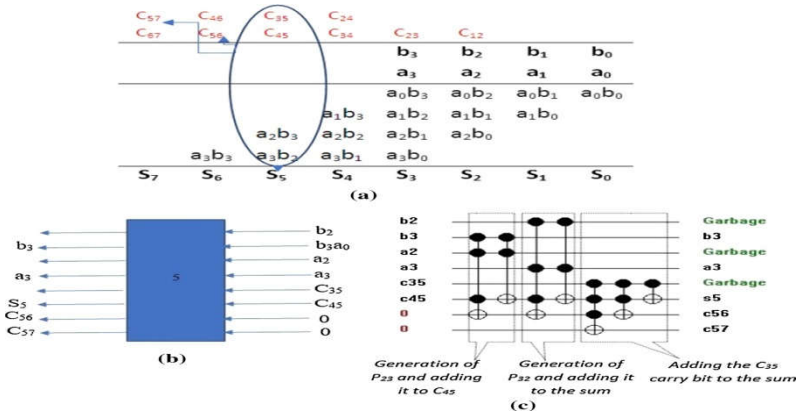

Fig. 9 Block Diagram of Reversible Circuit of Column 5

This the column wise operation for column 6 and block diagram and reversible circuit generated for column 6 multiplier.

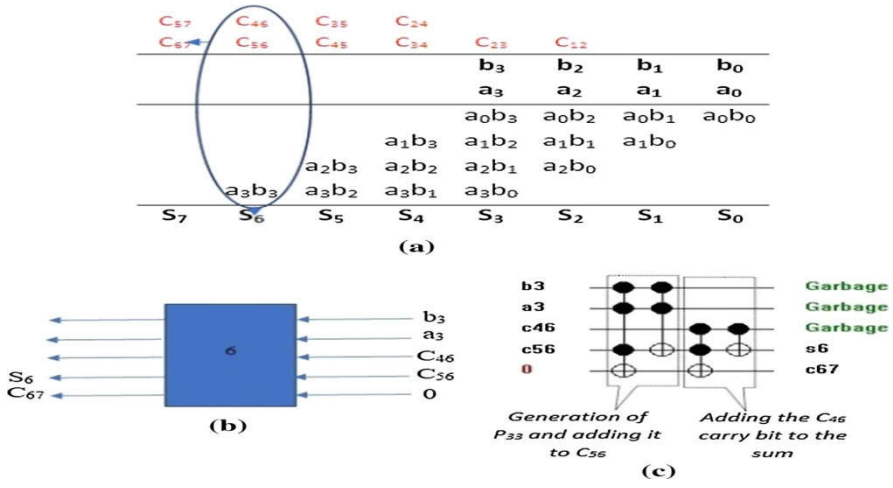

Fig. 10 Block Diagram of Reversible Circuit of Column 6

This the column wise operation for column 7 and block diagram and reversible circuit generated for column 7 multiplier.

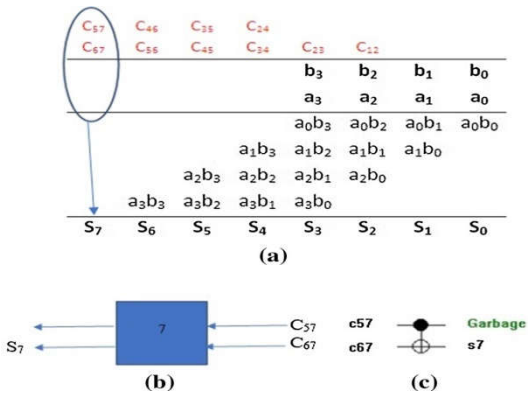

Fig. 11 Block Diagram of Reversible Circuit of Column 7

4. RESULTS AND DISCUSSIONS

4.1 Evaluation and Comparison

The reversible circuit for a column multiplier is proposed. A reversible circuit has two characteristics i.e., the number of inputs and outputs of the circuit are equal and there is a one-to-one relationship between input and output combinations which is shown in fig.13 In order to design a reversible circuit or convert a classic circuit into a reversible one, two characteristics must be produced in it. A reason for adding garbage outputs to the circuit is to make it reversible. If the number of equal output combinations in a circuit is not more than 2^n, using the minimum n garbage outputs can create a one-to-one characteristic in the circuit soin this proposed multiplier the number of garbage outputs to reduce twelve which is shown in fig 13.

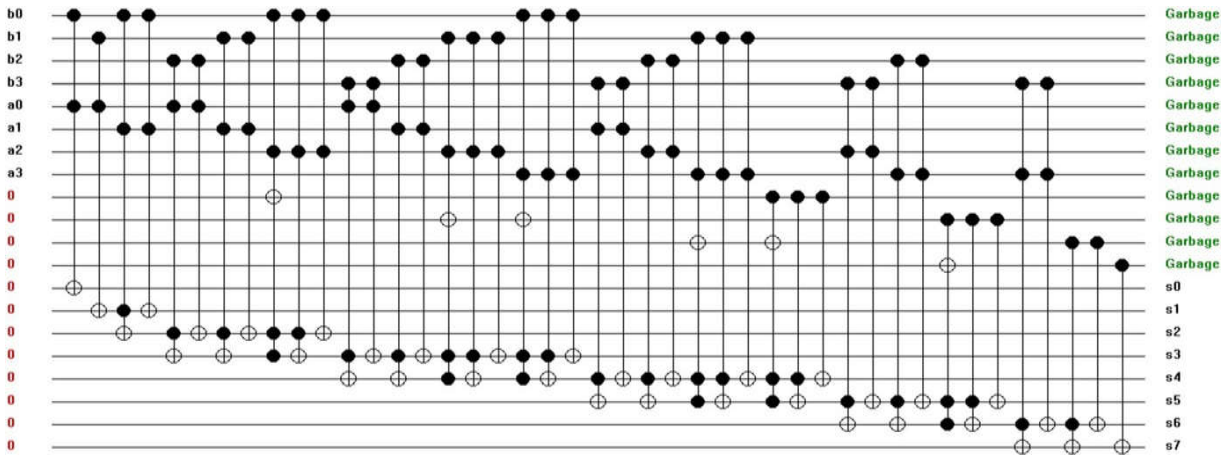

Fig. 12 Reversible Circuit for a Column Multiplier

Table 2 represents the maximum number of equal output combinations of each proposed multiplier block and the minimum number of garbage outputs required to make the block reversible. As can be seen in all eight blocks above, the number of used garbage outputs is lowest possible one

Table 1: Number of Garbage Outputs Required to make the Proposed Multiplier blocks Reversible.

Column No.	No. of required Garbage Outputs	No. of main Outputs	Total No. of Outputs
0	0	3	3
1	0	6	6
2	0	9	9
3	2	9	11
4	3	7	10
5	3	5	8
6	3	2	5
7	1	1	2
Total	12	42	54

In table 4 it compares the garbage outputs, ancilla inputs, number of gates and the quantum cost of the circuits presented by others to the proposed circuit. The main aim of the proposed circuit is to reduce the number of inputs and outputs, quantum cost, partial products and garbage outputs

Table 2: Comparison of different Reversible Multipliers

Design	Quantum Cost	No. of Gates	Garbage Outputs	Ancillia Inputs
[1]	505	53	22	52
[2]	140	32	40	40
[3]-Design 1	135	32	28	36
[4]-Design 1	N/A	N/A	22	23
[4]-Design 2	N/A	N/A	24	26
[4]-Design 3	140	28	32	32
[5]- Design 1	137	28	31	31
[5]- Design 2	N/A	N/A	14	14
[6]- Design 1	N/A	N/A	17	17
Proposed Design	402	43	12	12

CONCLUSION

This work has proposed a column-wise structure for multipliers. In this structure, unlike most other works in the field of reversible multiplier implementation, which consider separate blocks to generate and add partial products, computational operations for multiplying two numbers are investigated at the stage of the columns of multiplication. This greatly reduces the number of blocks making up the multiplier, resulting in a significant reduction in the number of ancilla inputs and garbage out-puts. The mentioned blocks are also designed in such a way that the main multiplier inputs pass through them without any change. This feature eliminates the need forusinga separate circuit to generate the fan-out.

The number of ancilla inputs in previous works ranged from 23 to 36. Moreover, the number of garbage outputs used in those works ranged from 22 to 32. Using the proposed method, the number

of ancilla inputs and garbage outputs was reduced to12 by lowering the number of multiplier blocks. The number of multiplier ancilla inputs and garbage outputs was improved using this method by 14–66%, compared to previous works. Infact, the focus of the current paper was on reducing the size of the multiplier circuit, which was reduced by 9–55% compared to previous works. The circuit size refers to the total number of inputs and outputs of the circuit, include main and ancilla inputs, and main and garbage outputs. In order to compare other cost metrics in this work with others, the proposed method was used to synthesize reversible circuits. This method provides a definitive, but not optimal, answer for each truth table. A 4 × 4 reversible multiplier with eight ancilla inputs and eight or more garbage outputs, synthesized using this method, has a quantum cost of 5076, which is high and unreasonable. By reducing the number of ancilla inputs and garbage outputs to 12

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