DESIGN AND IMPLEMENTATION OF HIGH-SPEED TERNARY SRAM CELL IN CNTFET

Dr.R.Manoj Kumar[1], K.M.S.G.Pragnya[2], K.Divya Bhanu[3],K.Pradeepthi[4], P.Hemasree[5] UG Students[2,3,4,5],Department of Electronics and Communication Engineering, Vignan'S Institute of Engineering for Women

Dr.R.ManojKumar[1], Associate Professor, Department of Electronics and Communication Engineering, Vignan'S Institute of Engineering for Women

ABSTRACT

The purpose of the project is to provide a solution to a large-scale delay problem of SRAM cells without degrading cell stability and device reliability. SRAM has benefits in terms of operating speed where it is high, as a result, it takes less time for accessing data or information and it does not require periodic refreshment to maintain data. As the Ternary logic offers an advantage over binary logic by increasing bit density and energy efficiency, this logic in SRAM cells is constructed using two cross-coupled STIs where these STIs act as a data storage element, and the ternary logic circuits are based on complementary CNTFET design style which uses three different threshold voltages for their transistors. To access the efficiency of the different ternary SRAM cells, HSPICE simulations were conducted in the CNTFET with the Ternary logic.

Keywords: Standard Random Access Memory (SRAM), Carbon Nanotube Field-Effect Transistor (CNTFET), Ternary Logic.

INTRODUCTION

The digital electronics industry has advanced quickly, which has led to the shrinking of semiconductor industries. A promising method for creating effective low-power circuits is carbon nanotube technology. The Carbon Nano Tube Field-Effect Transistors (CNTFET) is indeed a 1998 invention that operates at the nanoscale. As CNTFET performs better than MOSFET, it can withstand higher temperatures and has a negligibly small impact on its threshold voltage. They are the most enticing replacement for standard transistors. They are anticipated to be three times faster than silicon-based transistors while using the same amount of power. The mechanical, thermal, and electrical conductivities of CNTs are incredibly high. They are most likely the best feasible electron field emitter. Ternary logic has recently received a lot of attention in VLSI designs due to several benefits it provides over binary logic. The complexity and quantity of connections may be reduced with ternary logic since each wire may handle more data than its binary counterpart for the same amount of data.

One more benefit of ternary logic is high-speed broadcast for serial and serial-parallel data. In electronics, static random-access memory—often used in microprocessors, microcontrollers, and computer applications—is a type of random-access memory that stores data in a static form if the memory has power. As this type of memory does not require dynamic refreshment, its cycle time is shorter. Its advantage is that, in comparison to other memory, it gives better performance. A typical SRAM cell may hold between 1MB and 16MB of data. Both the price and density are higher. Each

bit in a cell is stored in one of four transistors that are set up as cross-coupled inverters in the basic circuit for a single cell. The MOSFET transistors are employed in these circuits since they are a common SRAM chip and require a lot less power. Bipolar junction transistors and MOSFETs are two different types of SRAM chips.

LITERATURE REVIEW

Low power and high-performance ternary SRAM design are based on cycle operator in ternary logic andit is based on buffer using it leads to impractical results to have an exact size[1] . The ternary logic circuit based on negative capacitance fields exhibits non-destructive read and reliable write operations for all three states and due to additional transistors cell area increased[2] . The design of 17T CNTFET ternary s-ram cell adds an advantage to reducing the cell size as the power delay product is less,the energy efficiency increases[3] .In carbon Nanotube SRAM performance evaluation the static power consumption of CNTFET SRAM cell are improved with stability[4]. SRAM-based ternary content -addressable memory for FPGAs uses single-bit parity to detect faults at a minimal cost of logic and critical path delay provides protection against soft errors with better response time but it consumes more power and lacks in required flexibility[5]. NOR-SRAM with wider reference voltage intervals, improves accuracy in linear quantization schemes. This improvement is shown by employing an XNOR-SRAM but due to the presence of threshold voltage drop,it affects the switching delay[6].

The resource-efficient SRAM-based ternary content addressable memory increase in memory efficiency at the cost of a reduced through put where as it takes more time to switch between operations therefore, the system runs slower[7].

TERNARY SRAM CELLS

Ternary SRAM cell: The Ternary SRAM cell consists of two cross-coupled ternary inverters. By connecting ternary inverters back-to-back, a trit-storage elementis implemented as a ternary SRAM cell. READ and WRITE operations of the ternary are performed with the help of a sense amplifier Ternary logic is performed on three-valued logic and has received attention due to its advantage over binary logic such as increased bit density and energy efficiency.

These techniques are simulated and implemented using the HSPICE tool by writing the respective code in spice netlist.

General conditions for the delay :

write 0: For write 0 q will be equal to Vdd and qb is zero.

write 1: For write 1 q will be zero and qb will be Vdd.

In write 0 minimum percentage of q and the maximum percentage of wl will be calculated.

In write 1 maximum of q and the minimum percentage of wl will be calculated

TSRAM1 CELL

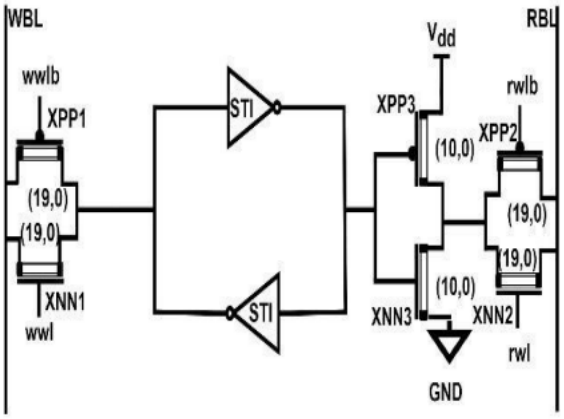

Figure 1 : TSRAM1 Cell[8]

The SRAM cell used a single-ended mechanism for read and write operations. The data is forced on the Write Bit Line (WBL) to write into the memory cell through the write transmission gates (MN1 and MP1). The read buffer consists of transistors P-CNFET and NCNFET, MP3,and MN3, respectively, with chirality (10, 0) and transmission and MN3, respectively, with chirality (10, 0) and transmission gates (MN2 and MP2). The RBL was pre-charged to 0.45V, and according to stored value, RBL was charged/discharged to 0.9V/0V or remained at 0.45V. Fig. 3. SRAM cell proposed in [8][11] (TSRAM 1) required a sense amplifier that can detect 0V, 0.45V, and 0.9V. This SRAM cell refers to TSRAM in this manuscript. Due to the single-ended functionality of TSRAM 1, the SNM improved with standby power consumption for '0' and '2' states, and the SRAM is free from the read-to-disturb problem.

Table 1 : Truth table of TSRAM1 Cell

operation	Read	Write
WBL	Vdd	0/ Vdd
wwl	0	Vdd
wwlb	Vdd	0
RBL	Precharge to Vdd	Vdd
rwl	Vdd	0
rwlb	0	Vdd

SIMULATED RESULT :

1. In write 0 condition the trigger wl, target q noted and less delay is obtained.
2. In write 1 condition the trigger wl, target q noted and less delay is obtained.

WRITE OPERATION OF TSRAM1 CELL :

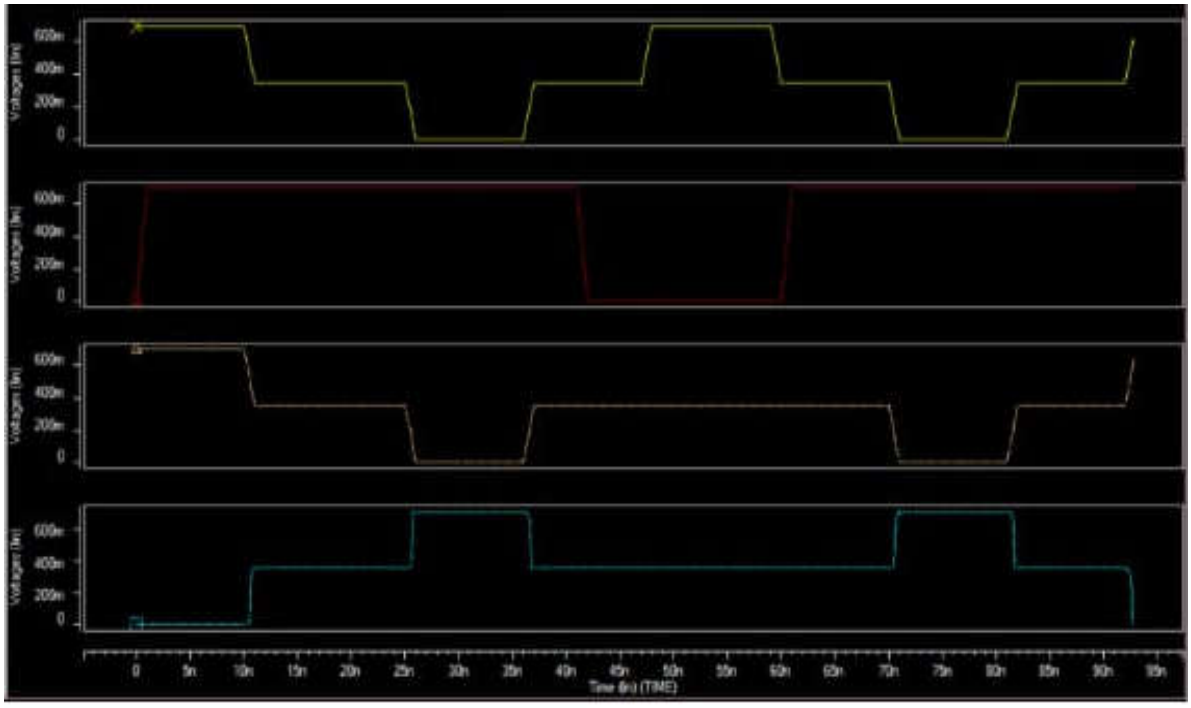

Figure1.1: Write operation of TSRAM1 cell [8]

READ OPERATION OF TSRAM1 CELL :

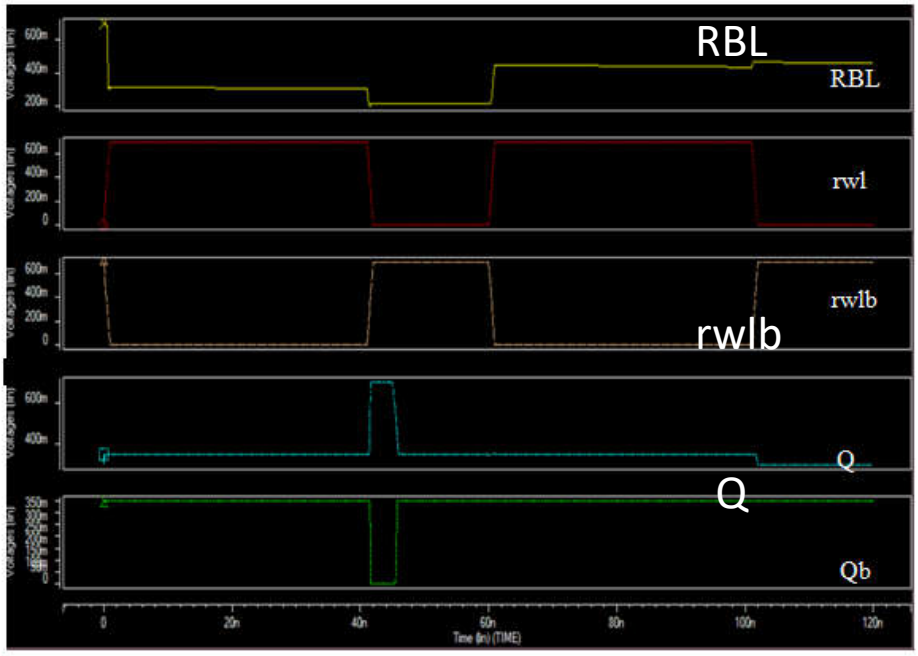

Figure1.2: Read operation of TSRAM1 cell [8]

TSRAM2 CELL

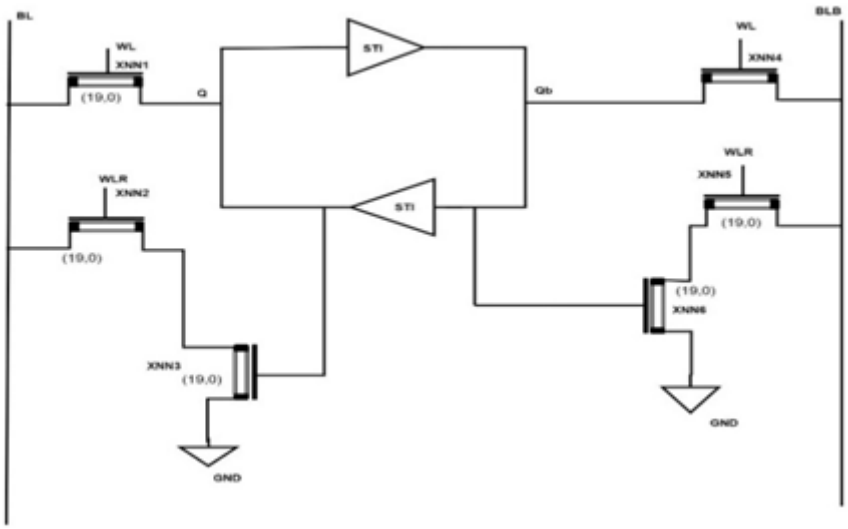

Figure 2: TSRAM2 cell [10]

Thechirality of the CNFETs was changed to improve the SNM and to reduce power dissipation in the 1st proposed SRAM of [10].By increasing the chirality of CNFET used in the ternary SRAM, read and write delay reduced .Although The SRAMs proposed in [10]improved the delay of storing the trits over TSRAM 1, here the delay is further decreases .

Table 2: Truth table of TSRAM2[10]

operation	Read	Write
BL	Vdd	0/ Vdd
BLB	Vdd	Vdd/0
wl	0	Vdd
wlr	Vdd	0

SIMULATED RESULT :

In write 0 condition trigger wl ,target q values noted and the the delay is obtained.

In write 1 condition the trigger wl,target q values noted and the delay is obtained.

WRITE OPERATION OF TSRAM2 CELL:

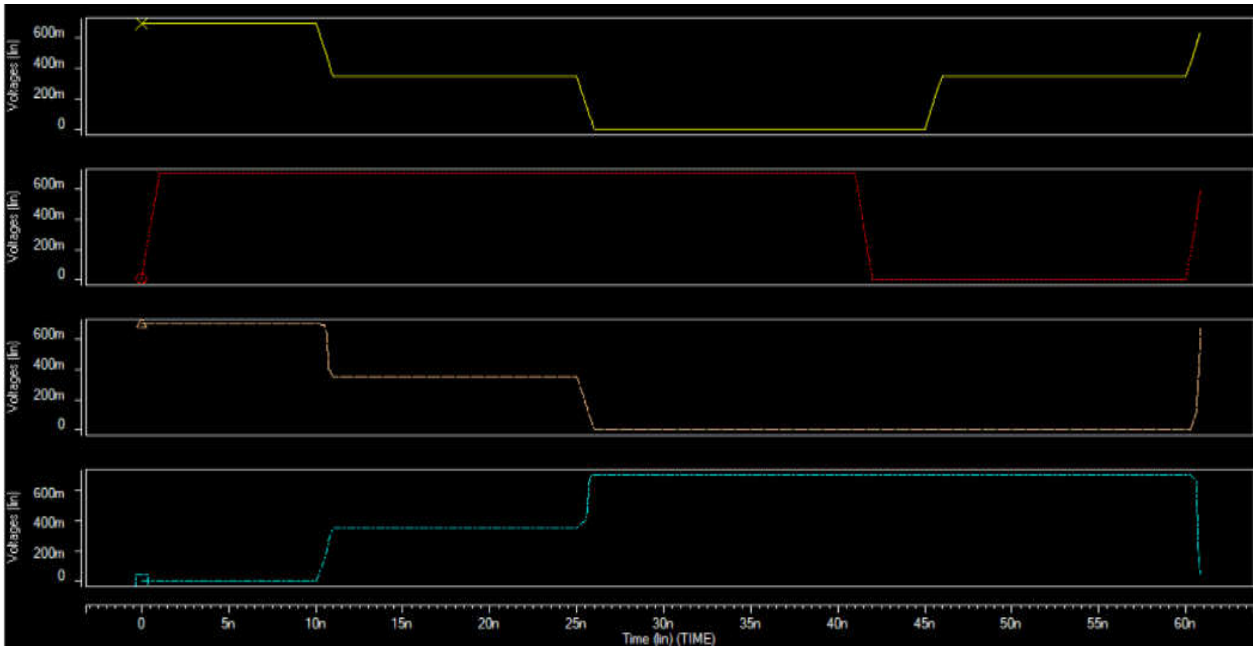

Figure 2.1: Write opertion of TSRAM2cell[10]

READ OPERATION OF TSRAM2 CELL

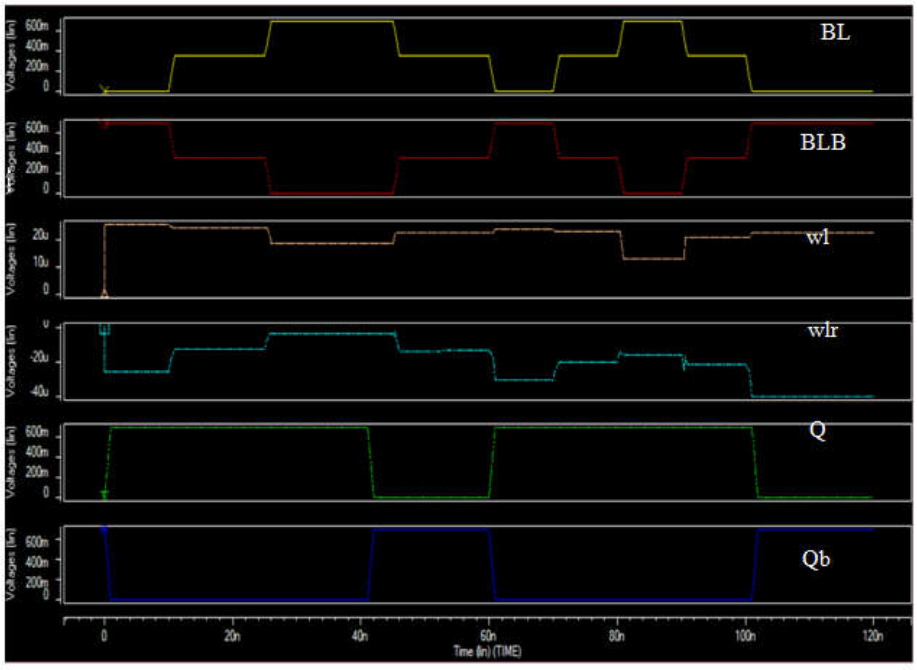

Figure2.2: Read operation of TSRAM2 cell[10]

TSRAM3 CELL

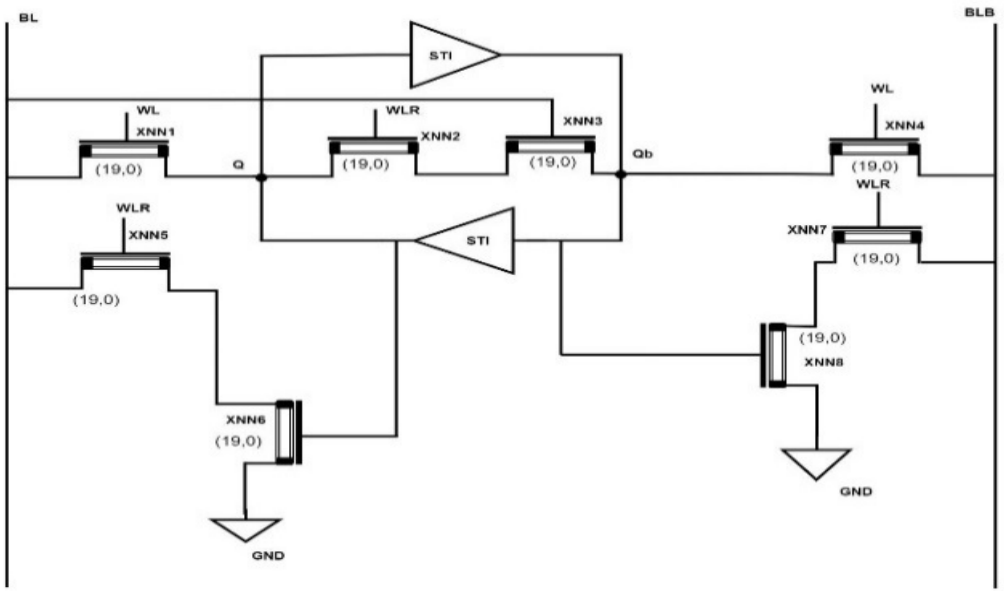

Figure3: TSRAM3 cell[10]

In the second proposed SRAM cell, two more transistors added, as shown in Fig. 3, to reduce the number of bit lines during the storage of trit '1'. The addition of transistors in the proposed 2nd SRAM of [22] caused a marginal increase in power consumption.The 2nd proposed SRAM of [22] refer as TSRAM2 in this manuscript .The traditional SRAM cells use back to back inverter to store the bit; additional pass transistors uses to read and write from memory cells. The ternary inverter STI proposed has two parts: one part contains four transistors, which activatedwhen input '1' is applied, the second part contains only 2transistors, and this part activated when the input is '2' or '0'.Here the the SRAM cell delay for input '1'reduces, and the memory cell's response becomes faster.

Table 3:Truth table of TSRAM3 cell[10]

operation	Read	Write
BL	0/ Vdd	0/ Vdd
BLB	Vdd	Vdd/0
wl	0	Vdd
wlr	Vdd	0

SIMULATED RESULT :

In write 0 condition the trigger wl , and target q values are noted and the less delay is obtained.

In write 1 condition the trigger wl,target q values are noted and the less delay is obtained.

WRITE OPERATION OF TSRAM3 CELL:

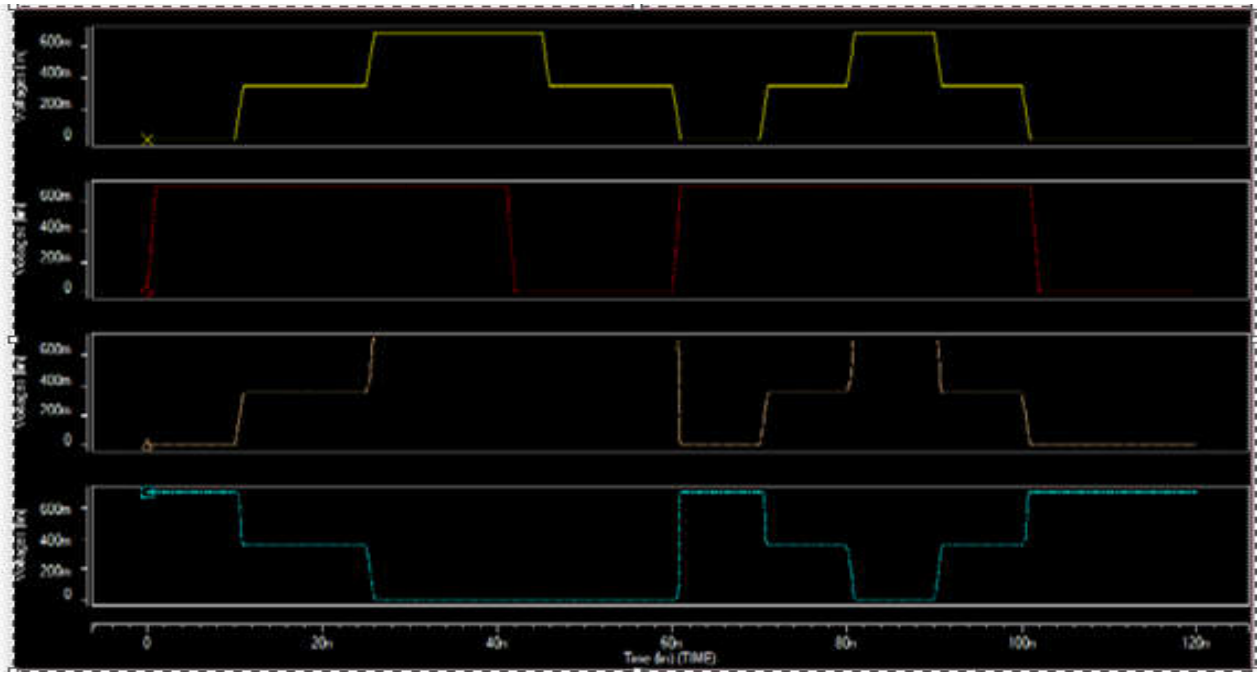

Figure 3.1: Write operation of TSRAM3 cell[10]

READ OPERATION OF TSRAM3CELL:

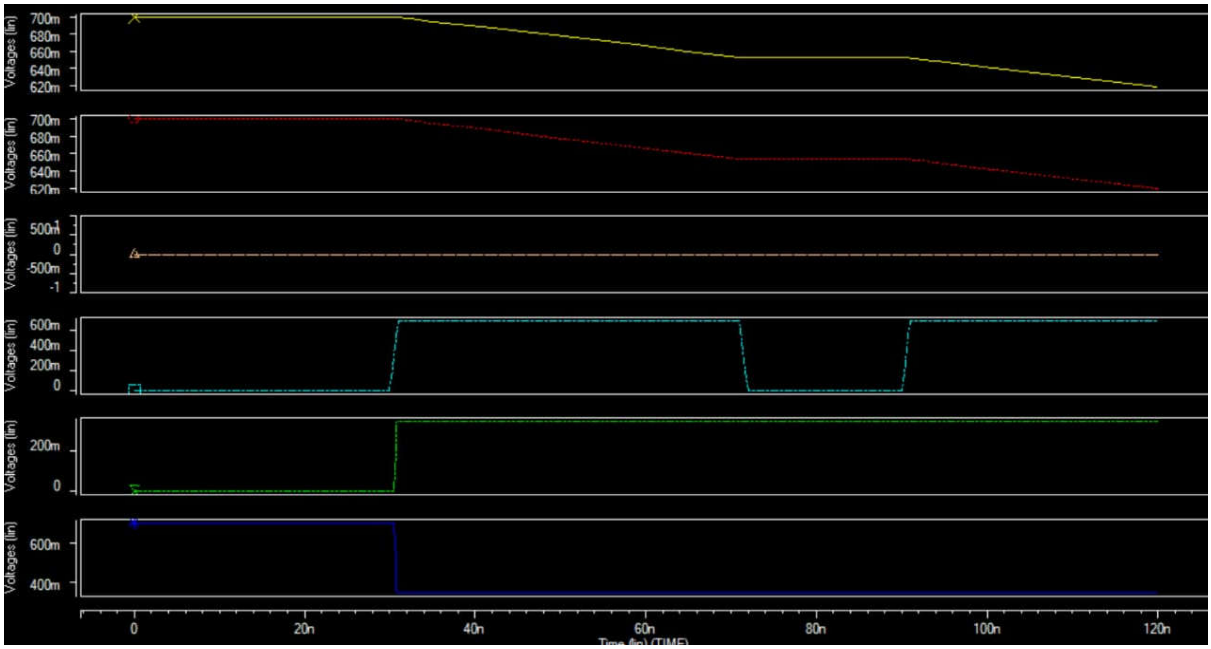

Figure 3.2: Read operation of TSRAM3 cell[10]

RESULTS AND DISCUSSION :

Table 4: Results of write operations

SRAM Cells	Write 0		Write 1	
	DELAY(nS)	POWER (uW)	DELAY (nS)	POWER (uW)
TSRAM 1	0.082	5.61	0.083	5.8
TSRAM 2	0.104	3.22	0.074	6.8
TSRAM 3	0.104	3.24	0.077	6.8

Table 5: Results of Read operations

Operations	Read	
1.	DELAY(ns)	POWER (uW)
TSRAM 1	0.319	0.0276
TSRAM 2	0.4	0.0106
TSRAM 3	0.104	0.0412

From the obtained result of fig 1 it is observed that the single-ended mechanism is used for read and write operation,therefore read disturb problem is avoided from Figure 2 The circuit results in more dissipation, and therefore the static noise margin performance becomes low.More number of circuits in Figure 3 results in increase the chip area which inturn leads to chip size therefore addition of transistor causes a marginal increase in power consumption.

CONCLUSION :

The three ternary sram cells are simulated and their power and delays are compared in both read and write operations . From the write operation ,the ternary sram1 is less delay when compared with ternary sram 2 and ternary sram 3.Ternary sram 3 gives better performance in read operation when compared with ternary sram1 and ternary sram2.Therefore ternary sram1 and ternary sram3 in write and read operations gives better result .

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