A HIGH SPEED VLSI ARCHITECTURE OF SQUARE ROOT BRENT KUNG CARRY SELECT ADDER

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ABSTRACT: VLSI technology is an emerging field in the current technological scenario due to its advancements in fields of systems architecture. Adders are the basic building blocks in digital integrated circuit based designs. Carry Select Adder is one of the important adders used for arithmetic operations. It is a high speed adder used in VLSI architectures but at the expense of area and power. In this paper, VLSI architecture of Square Root (SQRT) Brent Kung Carry Select Adder (BKCSA) is proposed using Binary to excess-1 converter to speed up the binary additions. In this paper, structure of 16-Bit Regular Linear Brent Kung CSA is designed along with the proposed Modified SQRT BK CSA design. The logic operations can be analyzed using a Binary to Excess-1 Converter (BEC) to study the data dependence and to identify the redundant logic operations. The experiments are carried out and the simulation is done using XILINX. The proposed work shows that proposed 16 bit SQRT Brent Kung Carry Select Adder has less chip area with slightly more delay and it is more efficient high speed adder among other architectures of CSLAs.

KEY WORDS: Carry Select Adder (CSA), Brent Kung (BK) adder and Binary to Excess-1 Converter (BEC).

I. INTRODUCTION

Very large scale integrated circuits the major problems found are more power consuming, slow working and taking large space in memory units it was generally observed that a system is required having low power consuming, High speed and less area. The design engineers are trying to design a system which can perform its best by giving high performance Parameters. The parameters are observed by trial and fault analysis the designs are tested and Fabricated [1]. In this research work we are focusing on adder circuit. If the delay is reduce than the speed can be increased. To have a best system it is essential to focus on all the parameters such as less area, low power, less time consuming, occupying less frequency and high speed. All this good performing system can be obtained if a hybrid adder structure is inserted in arithmetic unit.

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. Addition usually impacts widely the overall performance of digital systems and an arithmetic function. Adders are used in multipliers, in DSP to execute various algorithms like FFT, FIR and IIR. Millions of instructions per second are performed in microprocessors using adders. So, speed of operation is the most important constraint. Several algorithms have been presented for high speed parallel addition, and there is a trade-off between speed and area. Hence, binary adders are basic building blocks in very large-scale integrated circuits. Therefore fast and accurate operation of digital system depends on the performance of adders. Hence improving the performance of adder is the

main area of research in VLSI system design.

Design of low power, high speed data path logic systems are one of the most essential areas of research in VLSI. In CSA, all possible values of the input carry i.e. 0 and 1 are defined and the result is evaluated in advance. Once the real value of the carry is known the result can be easily selected with the help of a multiplexer stage. Conventional Carry Select Adder [5] is designed using dual Ripple Carry Adders (RCAs) and then there is a multiplexer stage. Here, one RCA (Cin=l) is replaced by brent kung adder. As, RCA (for Cin=O) and Brent Kung adder (for Cin=l) consume more chip area, so an add-one scheme i.e., Binary to Excess-l converter is introduced.

II. LITERATURE SURVEY

In this paper [4] investigates four types of adder PPA's (Kogge Stone Adder (KSA), Spanning Tree Adder (STA), Brent Kung Adder (BKA) and Sparse Kogge Stone Adder (SKA)). Additionally Ripple Carry Adder (RCA), Carry Look ahead Adder (CLA) and Carry Skip Adder (CSA) are also investigated. These adders are implemented in Very-log Hardware Description Language (HDL) using Xilinx technology Integrated Software Environment (ISE) 13.2 Designed Suite. These designed are implemented in Xilinx technology Vertex 5 Field Programmable Gate Arrays (FPGA) kit and delays are measured using Agilent 1692A logic analyzed and all these adder's delay, efficient power and area are investigated and compared finally.

In the paper [6] carry Select Adder (CSLA) is one of the good adders used in many computer data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for efficient the area and power consumed in the CSLA. This work used a simple and efficient gate-level modification to significantly efficient the area and power of the CSLA. Based on this modified 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture design has been developed and compared with the regular SQRT CSLA design architecture. The proposed design has reduced efficient area and power as compared with the regular SQRT CSLA with only a slight increased in the delay. This work evaluates the performance of the proposed implemented of designs in terms of delay, area, power. layout in 180-n CMOS process technology. The results analysis shows the proposed CSLA structure is much good than the regular SQRT CSLA.

In this paper [7] Carry Select Adder (CSLA) is one of the fastest adders used in processors to perform fast arithmetic functions. From the structure of the CSLA, it is clear that there is scope for efficient the area and power consumption in the CSLA. This worked uses a simpler and sufficient transistor level modification to significantly efficient the area and power of the CSLA. Based on this modification 4-bit design CSLA architecture have been developed and compared with the regulated CSLA architecture design. The proposed worked design has reduced power efficient area as compared with the regular CSLA with only a slightly increased in the delay. This work evaluated the performance of the proposed worked designs in terms of delay, area, efficient power, and their products by hand with logical effort and through custom design and layout in 180-nm CMOS technology file.

In this Paper [10] Carry Select Adder (CSA) is known to be the fastest adder among the conventional adder structures. It is used in many processors for realizing faster

arithmetic operations. In this paper, present an innovative CSA architecture. It employed a novel incremental circuit in the interim stages of the CSA. The proposed designed is done through designed and implemented of 16, 32 and 64-bit adder circuits. Comparisons with existing paper conventional fast adder design architectures have been made to prove its efficiency. The performance analysis shows that the architecture achieves three folded advantages in terms of delay, area efficient power.

III. PROPOSED DESIGN

A. Linear Brent Kung Carry Select Adder

The basic CSLA consists of two ripple carry adders (RCAs) and one multiplexer (MUX). To reduce the area and delay caused due to RCA in this structure, the RCA with $Carry_{in}$=0 is replaced by Brent Kung (BK) parallel prefix adder. This result in a structure called Linear BK CSLA. The 16-bit LBKCSLA consists of four groups of same size with BKA for $Carry_{in}$=0 and RCA for $Carry_{in}$=1. By using tree structure of BKA, the speed of addition operation is also increased.

B. Binary to Excess-1 Converter (BEC)

BEC is used in the carry select adder instead of ripple carry adder to reduce the number of logic gates which lead to reduction in chip area.

The Boolean expressions of 4-bit BEC are listed below.

(Note: ~ -> NOT, & -> AND, ^ ->XOR)

Sum4 = ~S4; (13)

Sum5 = S4 ^ S5; (14)

Sum6 = S6 ^ (S4 & S5); (15)

Carry6 = C6 ^ (S4 & S5 & S6); (16)

C. Modified Square Root Brent Kung Carry Select Adder

Modified Square Root Brent Kung Carry Select Adder has been designed using Brent kung adder for $Carry_{in}$ =O and BEC for $Carry_{in}$ =l and then there is a multiplexer stage. It has 5 groups of different size Brent kung adder and Binary to Excess-l Converter (BEC). BEC is used to add 1 to the input numbers. Less number of logic gates are used to design BEC as compared to RCA therefore it consumes less area. The block diagram of the 16-bit modified Square Root BK Carry Select Adder is shown in Figure (1).

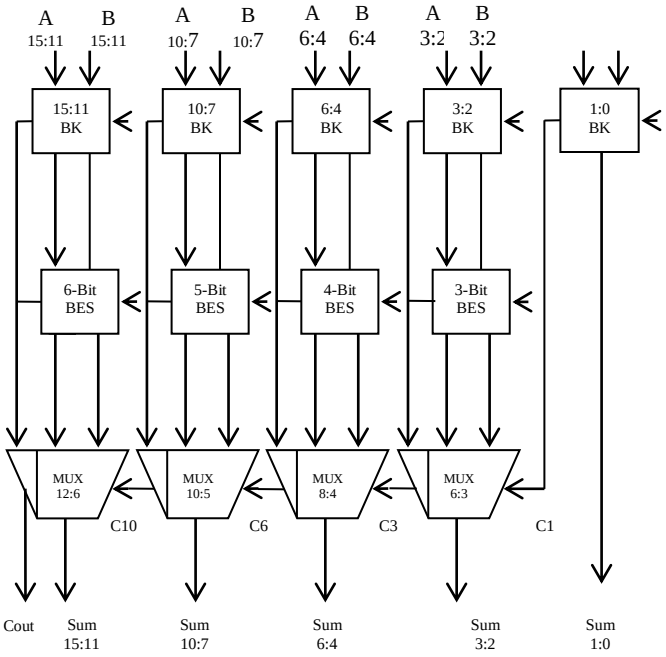

Fig. 1: BLOCK DIAGRAM OF 16-BIT MODIFIED SQRT BK CSA

Each group contains one BK, one BEC and MUX. For NBit Brent Kung adder, N+ 1 Bit BEC is used. Power consumption and delay of this adder is calculated for 16-Bit word size.

D. Binary to Excess-1 Converter based Brent-Kung CSLA

Modified Binary to Excess-1 Converter based Brent-Kung CSLA has been designed using Brent Kung adder for first four bits and C_{in}=0 and BEC for C_{in} =1 and then there is a multiplexer for selecting the sum bits

based on the carry bits. BEC is used to add 1 to the input numbers. Less number of logic gates is used to design BEC and thus consumes less area than the Brent-Kung based CSLA. Fig . shows the block diagram of 8-bit BEC based Brent-Kung CSLA.

IV. RESULTS

The simulation results for LBKCLSA and Modified SQRT BKCLSA of 16-bit using XILINX 12.2 software tool are shown in Figure (2). If inputs (i.e. A and B) for these two adders are "1111111111111111" and "1111111111111111". The outputs of summation and carry of these adders are "1111111111111110" and "1" respectively.

(a) Linear BKCSLA

(b) Modified SQRT BKCSLA

Fig. 2: SIMULATION RESULTS

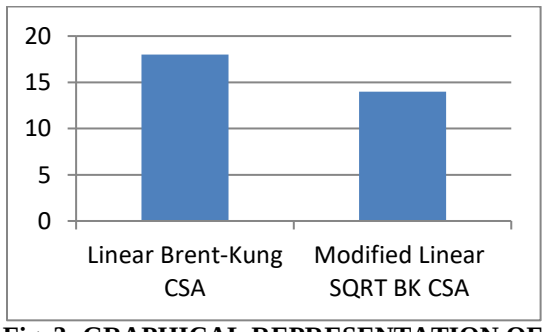

Fig. 3: GRAPHICAL REPRESENTATION OF TOTAL DELAY

Delay of, Linear Brent-Kung CSA and proposed Modified Linear SQRT BK CSA based on Binary to Excess-1 has been calculated. The graphical representation of comparison of delay of different adders is shown in Figure (3). It is evident that BEC based SQRT BK CSLA has reduced delay than all other adders.

V. CONCLUSION

In this work, a Modified Linear SQRT BK Carry Select Adder is proposed which is designed using single Brent Kung adder and Binary to Excess-l Converter to reduce the delay and power consumption of the circuit. Here, the adder architectures of Regular Linear BK CSA and proposed adder are designed for 16-Bit word size only. The synthesized results show that power consumption of Modified SQRT BK CSA is reduced in comparison to Regular Linear CSA but with small speed penalty. The both adder architectures were simulated using Xilinx software. The Chip Area and delay evaluations are also calculated for Modified SQRT BK CLSA and Linear BK CLSA and a comparison is done. The results show that Modified SQRT BK CLSA has occupying less area with slight increase in delay unit compared to Linear BK CLSA. It can be concluded that Modified SQRT BK CLSA is better when compared to other adders.

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