"Analysis of Cascaded Multilevel Inverter based Transformer Less Traction drive"

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Abstract—Multilevel inverters when supplied from equal and constant DC sources does not have a practical sense of applications. For each of the specific harmonic profiles the variation of the DC sources affects the values of the switching angles. This increases the difficulty of the harmonic elimination's equations. This paper presents the application of the cascaded asymmetrical multilevel inverter in the railway traction drive. The total harmonic distortion (THD) reduces with the increase in the voltage level. Various modulation techniques such as Phase Shifted Modulation (PSM), Level Shifted Modulation (LSM) and Selective Harmonic Elimination Techniques (SHE) were implemented in order to find the best modulation techniques among them. Also it is shown that SHE technique resulted in low THD. Thus, an IGBT based-cascaded five level asymmetrical inverters with SHE method has been modeled to lower the supply voltage to a level convenient for the traction induction motors.[1]

Keywords— multilevel inverter, PWM, electric traction, THD

INTRODUCTION

Steam and Diesel motors were thought to be a wellspring of ecological catastrophe on wheels. Therefore, there was a longing to enhance the efficiency and dependability of the steam footing commute[2]. This lead to the electrification of the railroad framework. Electric footing commute has now been thought to be an ancient method for transmitting energy to the traction motor that can convey as much as 2 times the tractive force yield of comparable diesel traction. It has high energy to-weight proportion which brings about speedier AC celeration and higher tractive effort. Due to enhanced speeding up, additional stations can be presented with less time delay and henceforth, a gift to the minor stations. There can be a further increment in the efficiency through regenerative braking by reusing the vitality of the easing off train in the plummeting slope. While sliding a slope, vitality can likewise be dispersed by the on-board resistors as warmth. The enhanced general execution and less vibration brings about quicker, more solace capable, smoother and calmer voyages for the travelers. The electric footing drives obliges medium voltage and high power operation. This can be accomplished with the help of multilevel inverters. The footing transformer ventures down the centenary voltage to a level helpful for footing engines[3]. This massive transformer lessens efficiency; add to weight, cost and The changing situation of the force interest of the world has lead to the advancement of different new power converters and new power semiconductor devices. One of them is the multilevel converter innovation that has been essentially presented for mechanical application having medium voltage and high power prerequisite.[1]

ELECTRIC TRACTION DRIVES

An electric locomotive is powered by electricity from overhead lines, a third rail or onboard energy storage such as a battery or fuel cell. Electric locomotives with on-board fuelled prime movers, such as diesel engines or gas turbines, are called as diesel-electric or gas turbine-electric locomotives because the electric generator/motor combination serves only as a power transmission system. A railway electrification system supplies electrical energy to railway locomotives and multiple units so that they can operate without having an onboard prime mover. There are several different electrification systems in use throughout the world.[2]

Electric drive technology was progressively changed from DC motor drive with rheostat control to induction motor drive with inverter control especially in early 1990s. Railway Company could save maintenance cost of rolling stock by half

after introduction of the new technology. In large cities where transport density is relatively high, energy consumption of commuter trains also reduced drastically by regenerative brake in place of mechanical brake and by train weight reduction. As far as commuter multiple units are concerned, the three phase drives with one inverter feed several traction motors in parallel, say multiple motor drive, is much less expensive than ones of individual motor drive. This solution will be applied to more railway vehicles in future. If railway vehicle has possibility to make railway operation more efficient, one can use electrical brake that can minimize vehicle maintenance staffs and simplifies train operation. Introducing this technology, all brake force from the top speed to zero is generated electrically and there is no mechanical wear of brake materials

MULTILEVEL INVERTER

The term "multilevel inverter" was rooted years ago. Multilevel inverters offer various applications in voltage ranging from medium to high such as in renewable sources, industrial drives, laminators, blowers, fans, and conveyors. Small voltage step results in making the multilevel inverters withstand better voltage, fewer harmonics, high electromagnetic compatibility, reduced switching loss, and better power quality[5].

Cascaded multilevel inverters were developed in the initial stage. Later, diode-clamped MLI'S were developed followed by flying capacitor MLI'S. These three topologies utilize different mechanisms to produce the required output. The topology introduced first, that is, the CMLI, is simply series connection of H-bridges.The diode-clamped MLI uses series capacitor bank whereas ,inflying capacitor mli,floating capacitors are used in order to clamp the output voltage [6].Hbridge inverters have isolation transformers, and then H-bridge cascaded MLIS were introduced to separate DCinput sources. But they do not need either clamping a diode or flying capacitors. Absence of voltage imbalance is the main advantage of cascaded mli. Fewer components are used in CMLI compared to diode-clamped and flying capacitor mlis [2–4]. Most of the researches are carried out in cascaded MLI configuration. But still the new trends are involved in the evolution of renewed multilevel inverters. Modifications are made in its inbuilt structure. A 7-level MLI was generated with 9 switches reducing 3 switches from the main conventional CMLI [5]. It offers good results yielding desired a 7level output with low THD. A 7 level MLI with 7 switches reducing 2more switches from the previous topology made a far improvement in the investigation of the switch reduction [6].Yet another topology of 7-level MLI was configured with 4dc sources and just 6switches to get 7-level output[7].The latter made a drastic move in topology development since the THD is low, and gate circuits used to drive the switches are less

It is mentioned everywhere that simplicity is the main advantage of CMLI to generate 5 levels using 8 switches, 7 levels with 12 switches, 9 levels with 16 switches, and so on [2–4,8].It clearly reveals that an increase in levels demands more number of switches. Then the comment on simplicity of CMLI is simply contradictory. Hence, the focus was eyeing on a real solution to this problem, that is ,how to simplify the complex circuit. Then arise the concept of "switch reduction". Exploring the existing topologies on basic 7 level, switch reduction was made from 12 switches to10, 9 gradually to 7 and then to 6.

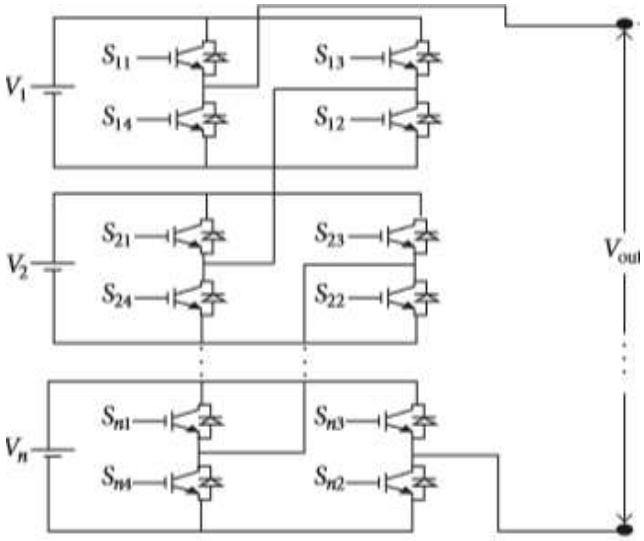


Figure1:Conventional cascaded n-levelMLI.

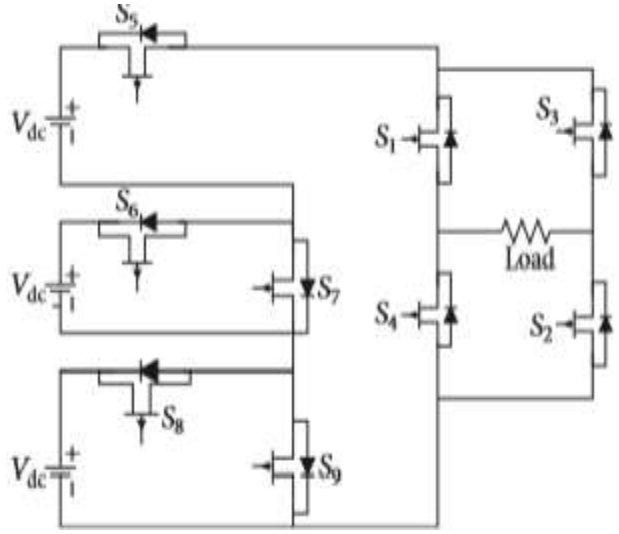


Figure2:7-level9-switchtopology

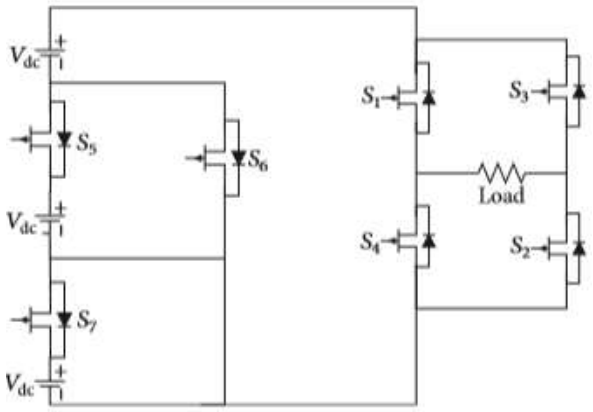


Figure3:7-level7-switchtopology

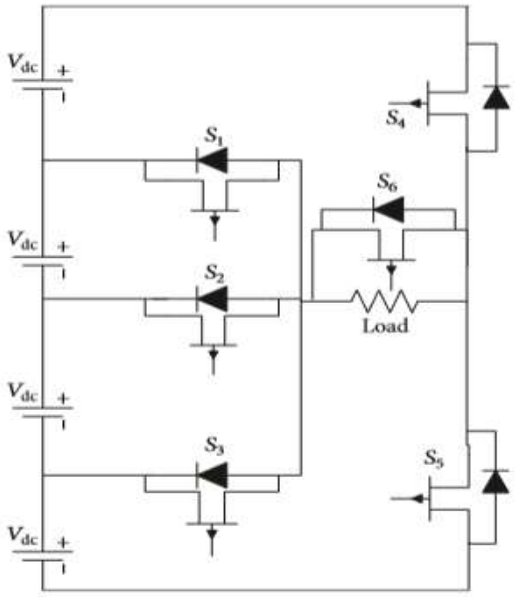


Figure4:7-Level6-switchtopology

Aiming at reducing the switches to the maximum possible extent and reducing complexity, the new topology is introduced with 5 switches for 7 levels, and this would be the least possible reduction. The new MLI configuration is made of 5 switches eliminating 1 switch from the existing 6 switches, 7-level topology [7] in a special arrangement with 4 inputs DC sources to generate 7 level output. The less switches we use lessen the cost of circuit building. The circuit credibility is checked without using pwm. Then identifying the effectiveness in working simulated the circuit with PD, POD, and APOD using MATLAB/SIMULINK.

(1) Conventional Topology. Using 3 DC voltage sources, 3 H-bridge units each with 4 switches together forming 12 switches in total are used in conventional CMLI which is representedinFigure1.Generalexpressionforoutputvoltage levels, $m = (n + 2)/2$ where n is the number of switches the configuration.EachBridgeisoutputting3Levels,+Vdc, 0, −Vdc. Cascading 3 Bridges in such a fashion to produce stepped 7 level staircase waveforms.

(2) Existing Topology

(a) 7-Level, 9 Switches. This topology which is shown in Figure2 is built with 3 dc sources, 1 H-bridge composed of 4 switches and then additional 5 more switches for producing stepped 7 levels, for positive andnegativehalfcycles.Table1 represent the switching scheme for this topology.

(b) 7-Level,7 Switches.Thistopologyismadeof7switches and 3 dc sources and is shown in Figure3. One H bridge present in the topology is mainly for polarity change. Here, three switches conduct at a time for level generation. The switching scheme is given in Table2.

(c) 7-Level, 6 Switches. This is a special configuration consisting of four dc sources and six switches. One switch across the load is used for zero level.S1, S2, S3 used for level generation and S4, S5 switches for polarity changing Figure4 represent the 7-level 6-switch topology and the corresponding switching patternisgiveninTable3.

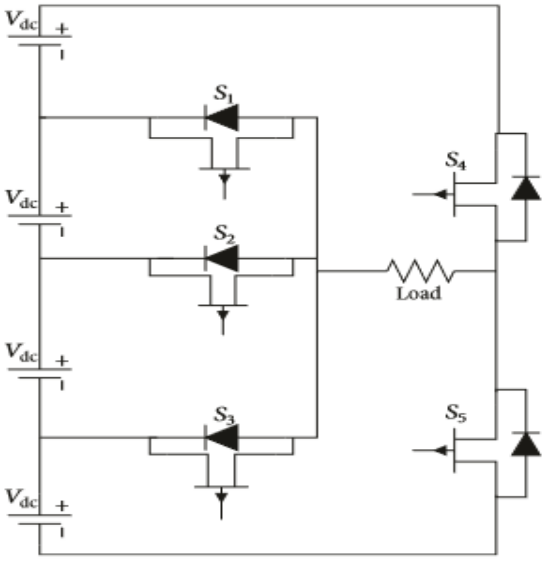


Figure5:7-level5-switchproposedtopology

(3)Proposed Five-Switch Topology.

The proposed 7 level MLI as shown in Figure 5 is about redesigning of existing 6-switch topology eliminating 1 switch attaining the tag of 5 switch configuration. The circuit thus obtained is the simplest design compared to conventional and all other existing topologies. It consists of four dc sources of 7 levels, for9-level, 5dc sources and soon. Generalized expression for output voltage levels for the new topology propose dis $m = (2 * n - 3)$,where m=number of output voltage levels, n=number of switches $m = (2 * V - 1)$,where V = number of dc sources. The design of pulse generation circuit makes the topology differ from others so as to obtain

the unique pulse pattern to trigger the switches attheproperinstant.SwitchesS1,S2, and S3 need to be compulsorily unidirectional or else the output waveform will get distorted. Reduced switches make the circuit compact and user-friendly. Though the usage of 4 dc sources for the generation of 7-level MLI results in less utilisation of sources, switch reduction benefits in low switching losses. No H-Bridge is used. Just 2 switches play the role of polarity reversal.Table4 represent the switching scheme for the proposed topology.

SPWM OF A SINGLE PHASE H- BRIDGE INVERTER

The basic SPWM techniques are unipolar pulse width modulation and bipolar pulse width modulation which are used in a single phase H –bridge inverter to vary its output voltage. [8]

***A. Bipolar Pulse Width Modulation*:** In this modulation, the gate pulses are obtained by comparing a sinusoidal modulating signal or reference signal with a high frequency carrier signal.

B. Unipolar Pulse Width Modulation: The unipolar modulation normally requires two sinusoidal modulating waves, which are of same magnitude and frequency but 180 degree out of phase. The inverter output voltage switches either between zero and +Vd during the positive half-cycle or between zero and –Vd during the negative half-cycle of the fundamental frequency. This modulation is also possible with two triangular carrier waves and one sinusoidal modulating signal.

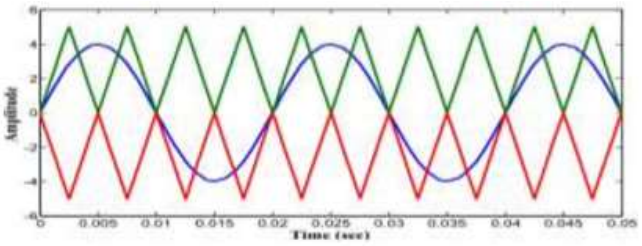


Fig. 6: Unipolar Pulse Width Modulation

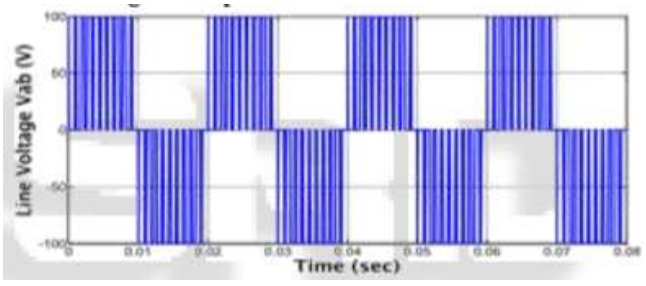


Fig. 7: Waveform for Unipolar Pulse Width Modulation

MULTICARRIER PULSE WIDTH MODULATION TECHNIQUES

The carrier based PWM techniques for cascaded multilevel inverter can be broadly classified into: phase shifted modulation and level shifted modulation. In both the techniques, for an m level inverter, (m-1) triangular carrier waves are required. And all the carrier waves should have the same frequency and the same peak to peak magnitude.

1) Phase shifted pulse width modulation.
2) Level shifted pulse width modulation.

In phase disposition PWM -In this modulation, all the triangular carrier waves are in phase.

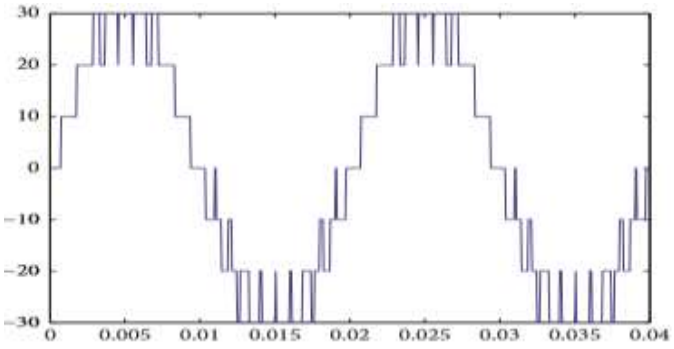
Phase opposition disposition PWM - In this form of modulation, the carrier waveforms are in all phases above and below the zero reference value. However there is 180 degrees phase shift between the ones above and below zero respectively.

Alternate phase opposition disposition PWM - In this form of modulation, the carrier waves are displaced from each other by 180 degrees alternately. In LS-PWM, each carrier is associated with the gating signals of NPC converter whereas in PS-PWM, a pair of carriers is associated with each cell of the CHB and FC converters. Because of the phase shifting of the carriers, power is evenly distributed among the cells which results in the smooth operation of CHB and the natural voltage balancing of the FC. Therefore, LS-PWM is mainly used for NPC converter whereas PS-PWM is practically used for CHB and FC converter. Even though IPD PWM results in low THD as compared to PS-PWM, the small difference in the high frequency content can be filtered out.

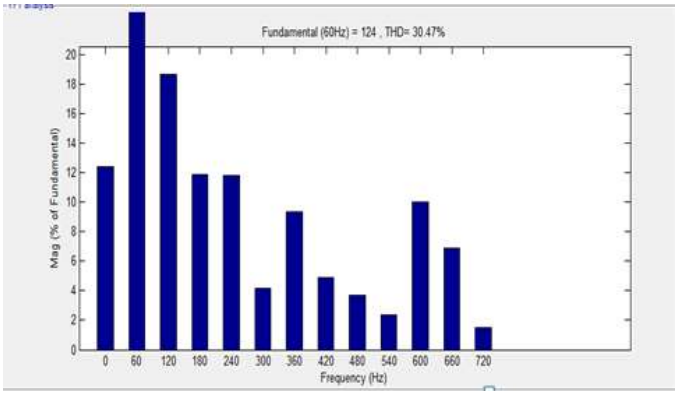
Selective Harmonic Elimination (SHE) Modulation Technique

SHE PWM is an optimizing algorithm that gives a superior harmonic performance in high power applications with the minimum switching frequency. As compare to other PWM topologies, only the SHE-PWM based techniques work effectively at low switching frequencies and theoretically provide the best output voltage and current quality. However these techniques suffer from a heavy computational process. SHE is normally a two-step digital process. First step of this method is to solve a group of nonlinear equations based on criterion of eliminating selected harmonics at different values of modulation indexes. These equations are solved by a numerical analysis processes or Newton-Raphson methods. Second, the result, which is a set of gating angles typically stored in look-up tables for the gating controller. If the number of the harmonics to be eliminated is increased, the number of precalculated switching angles will be increased accordingly; then the look-up table requires very large memory space and therefore the gating data must be carefully set-up.

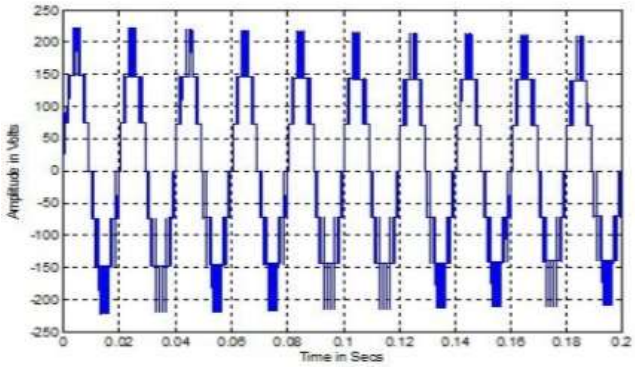
SIMULATION RESULTS - Various modulation techniques are implemented to simulate seven level cascaded H-bridge inverters in MATLAB-Simulink environment. These techniques are compared with each other to find the best modulation technique.



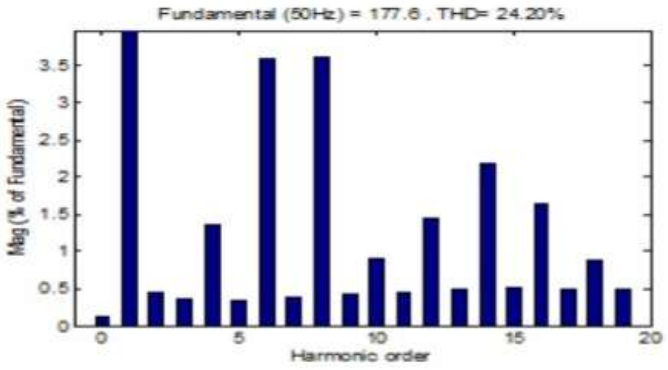
Output Voltage Waveform of seven Level Inverter



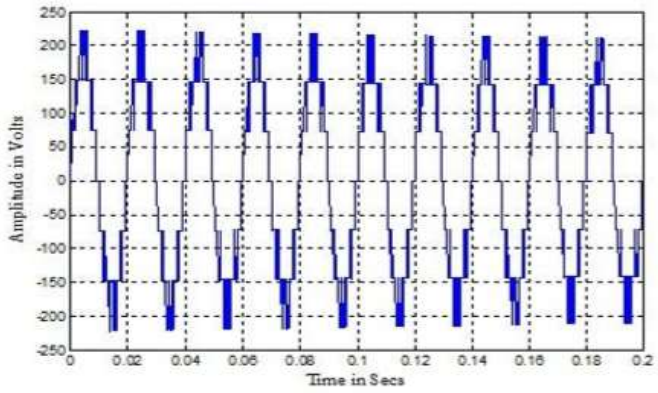
FFT Anaysis of seven level inverter



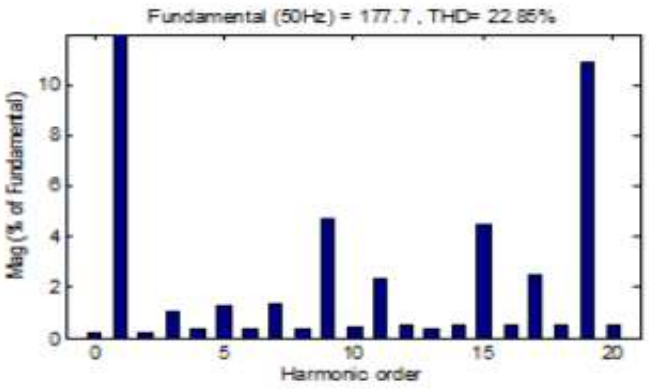
Output Voltage generated by PDPWM technique



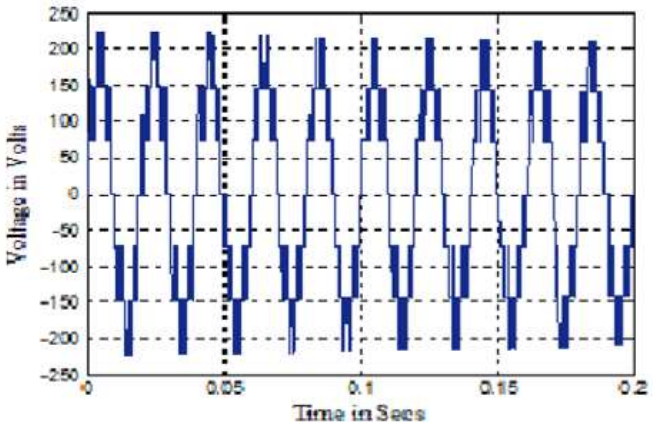
FFT plot for Output Voltage of PDPWM technique



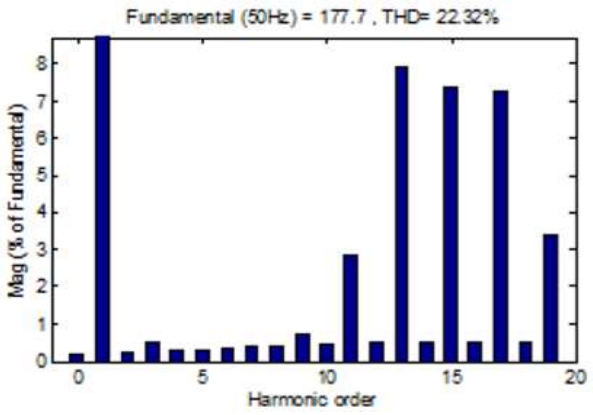
Output Voltage generated by PODPWM technique



FFT plot for Output Voltage of PODPW technique



Output Voltage generated by APODPWM technique



FFT plot for Output Voltage of APODPWM technique

COMPARISION OF THD VALUES IN (%) OF OUTPUT VOLTAGE OF SEVEN LEVEL CASCADED INVERTER OBTAINED BY IMPEMENTING VARIOUS MODULATION TECHNIQUES

Modulation type		THD in(%)	REMARK
Phase shifted PWM		24.67 %	
Level shifted	i.IPD	26.68 %	Phase shifted
PWM	method		PWM is better with low THD
	ii.POD method	25.89 %	
	iii.APOD method	27.52 %	

Comparing to two modulation techniques phase shifted PWM and level shifted PWM technique. The phase shifted pulse width modulation technique is better with low total harmonic distortion (THD).

CONCLUSION-

The seven level, cascaded H-bridge inverters were simulated in MATLAB/SIMULINK environment. Two types of Multicarrier Pulse Width Modulation-Level Shifted Modulation and Phase Shifted Modulation and SHE modulation technique were implemented for the cascaded multilevel inverter. The following things can be concluded about the modulation techniques and the multilevel inverters: Level Shifted Modulation was found to have better THD values as compared to Phase Shifted Modulation. Among the Level Shifted Modulation techniques, the In Phase Disposition (IPD) modulation technique was better in terms of THD. As the number of levels in the output voltage of the inverter increases, the synthesized waveform has more steps, which produces a staircase waveform that approximates to a sinusoidal waveform which is required. Also as the level of the output voltage increases, the harmonic distortion of the output Voltage waveform decreases. Selective Harmonic Elimination (SHE) Modulation Technique was found to be better in comparison to the above mentioned modulation techniques. The THD of the output line voltage of the seven-level inverter is comparatively low (less than 5%).

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