Implementation of Massive MIMO Systems for 512-Point FFT Processor using VLSI Technology

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Abstract: Substantial amount of latency in baseband is "Massive Multiple Input and Multiple Output"(MIMO) system. It establishes by new 5G technology and also by "Orthogonal Frequency Division and Multiplexing" -(OFDM). To proclaim latency of MIMO, a Fast Fourier Transform (FFT) is suggested. The Proposed System is to develop the VLSI chip routing technology to reduce no of computations and processing time and the main aim of this report is to decrease as many as butterfly operations in downlink .In FFT/IFFT ,memories occupied the chip area in uplink, which can be attained by registers. To wind up this process, a processor which is a 512-pt FFT is designed in MATAL and VLSI software.

Keywords - Massive Multiple Input and Multiple Output (MIMO), Orthogonal Frequency Division and Multiplexing (OFDM), Fast Fourier Transform(FFT), Latency , VLSI software, MATLAB Software

I. INTRODUCTION

In 5G New Radio (NR) "Massive Multiple Input and Massive Multiple Output"-(MIMO) technology is an integral element they consists of high amount of antennas at substratum terminal to upgrade spectrum efficiencies .Simultaneously supplementary antennas will help to improve the efficiency, power, throughput, delay. Due to high energy efficiency multicarrier guard band plays a predominant role for implementing the 5G new radio structure. Massive MIMO technology plays an extrusive role for upcoming challenges faced by the humans. Massive MIMO includes the use of energy consumption, decrease of delay, transcription of the media access control (MAC) layer.

To implemented a FFT processor which is used in communication. As we want to reduce the delay and to increase the speed as much as possible. These days technology is advancing day-by-day. So we have designed the FFT processor for 512 points.

This paper prime focus is on designing the 512-Pt FFT (Fast Fourier Transform) and also targeted the term Latency and implemented the FFT in MATLAB and Xilinx software. The main focus is to design the fixed 512 point for good communication between the users.

II. LITERATURE REVIEW

E. G. Larsson et al. [1] "Massive MIMO" plays a vital role for next generation communications systems. In this paper considered the large potential of "Massive MIMO" systems is a essential enabling technology for the coming beyond the 4G cellular and wireless systems. This system concentrated on the spectral efficiency, reliability robustness, and energy efficiency.

S. Liu and D. Liu [2] In this reference they mainly concentrated on a high efficient "Programmable Fast Fourier Transform" (P-FFT) processor has been developed for supporting variable points Fast Fourier transforms and discrete Fourier transforms(DFTs).

F Minotta[3] et.al This paper has some way to urge flexible FFT supported an address generation scheme for FPGA implementation, it introduced an algorithm and hardware to recreate the twiddle factors for the FFT radix-2 multiplication neglected the quantity of points, folding factor. In this reference they mainly focused on designing the FFT(fast Fourier transform and also it can achieve full hardware butterfly efficiency and no of adders are also reduced to half [4].

Wen-Chang Yeh [5] stated in the paper about a split-radix fast Fourier transform (SRFFT) pipeline architecture design. They have used the Cooley–Tukey-based algorithms for designing which is a regular and extensible for any 2^n –point. They presented an efficient combined SDC-SDF (Single-Path Delay Commutator-Feedback) radix-2 pipelined Fast Fourier Transform (FFT) architecture which has log2N-1 SDC stages, and 1 SDF stage [6]

III. PROPOSED SYSTEM

Some of the architectures designed the fast Fourier transform there are two types of architectures one is memorization based design and channel based architecture. In memory based number of processing elements is very high. Due to this delay occurs but our main aim is to design the fast Fourier transform processor with very low

delay. On the opposite side, the pipelined architecture has high throughput and low delay and price is very affordable

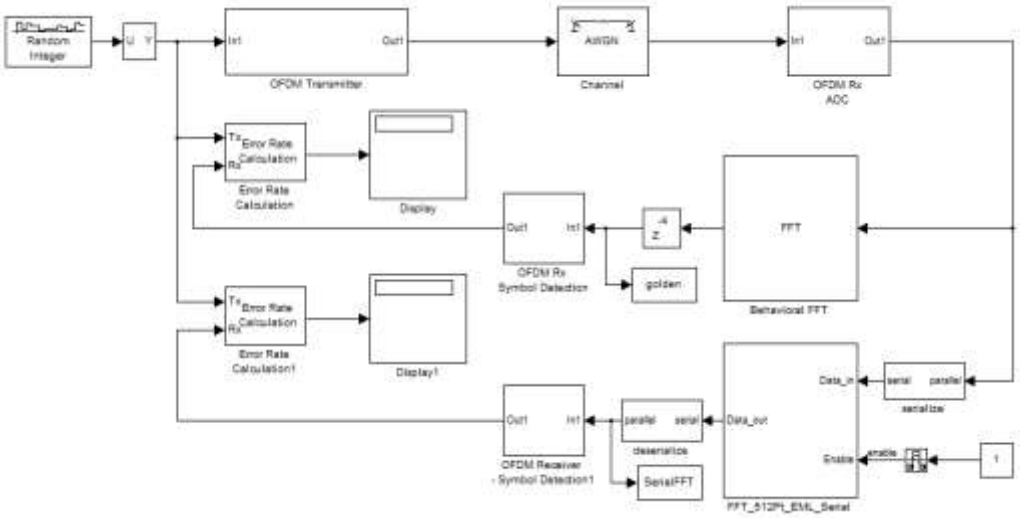


Figure1: Block diagram 512-Pt FFT processor

In this paper, we have to observe that they have used different architectures, algorithms and also been focused on a fixed point for designing a Fast Fourier transform (FFT) processor. With some extra modifications we designed a 512 point FFT and directly converted the simulink block diagram into required HDL synthesis code.

In this we used both VLSI software i.e Xilinx and MATLAB software. To know exact values of the latency we have designed 512 points and calculated the maximum delay and memory usage of fixed 512 points

In this system we are utilizing the multicarrier and multiplexing for transmitting the multiple antennas and receiving multiple antennas. The multicarrier modulation attenuates the original symbol with a time period of Ts but the time period length has been expanded to 512-Pt by transferring all symbols in an aligned form. Some part of the latency has been introduced by the "Orthogonal Frequency Division Multiplexing" (OFDM) Modulation in MIMO systems. To expand the low delay demand in integrated massive MIMO OFDM systems, A Fourier Transform processor is constructed, which diminishes the processing time delay of multicarrier based systems respectively.

The proposed structure using OFDM guard bands reduces the computations for implementing the 512-point FFT Processor, It leads to diminishing in the latency compared to the corresponding channel schemes.

To implement Massive MIMO System a modified channel construction with memory structure and also efficient statistics scheduling scheme for various memories and butterflies operations are implemented by using the VLSI technology integrated with multiple inputs and multiple outputs called massive MIMO systems . Using this, a 512-point FFT/IFFT processor design accomplish the minimum latency than for a simple pipelined FFT/IFFT construction.

IV. THE METHODOLOGY OF THE PROPOSED SYSTEM

The multicarrier guard bands helps for minimizing the channel noise and to produce the error free channel and it consists of numerous antennas at sender and also at receiver.

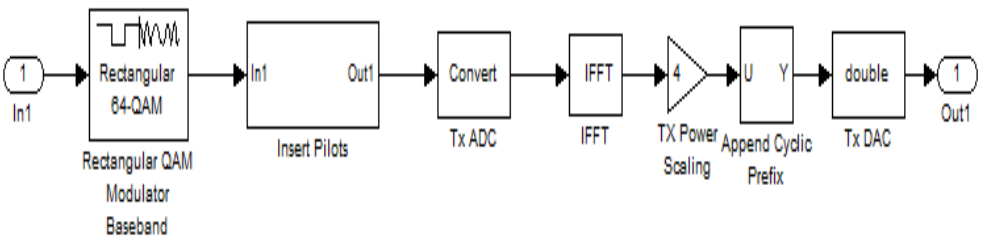


Figure2: OFDM Transmitter

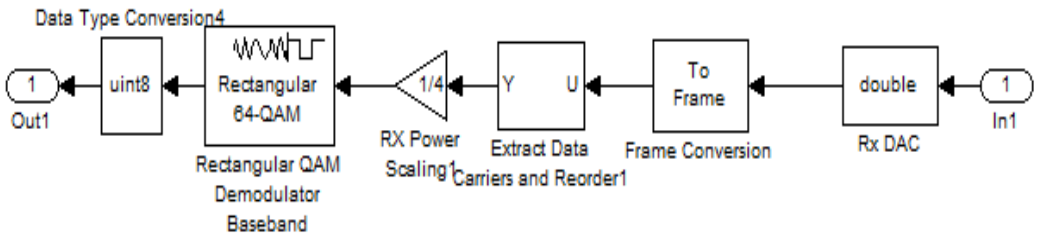


Figure 3: OFDM Receiver

4.1 Proposed Less Computational Delay for FFT

The guard bands are fully exploited for reduction of delay. To know how multicarrier system works, it's necessary to arrive at the acceptor. This acts as a heap of demodulators, converting each and every carrier all the way drop to DC. the equivalent demodulator also extracts the opposite carriers due to the carrier formation adequate the interchangeable of the design period defines that they have an entire amount of cycles within the design period and there's no interference contribution .And you can observe from the results of low delay for FFT

4.2 Proposed 512 –Point FFT

In the proposed scheme our main aim is to design the 512-point i.e fixed point and FFT is used to alter the time range to frequency range and this leads to low delay and also no of clock cycles are also calculated. In order todecrease the no of computations and time delay according to that the cost also reduces. The corresponding results and observations are discussed in chapter 5.

4.3 Less Delay Reordering Scheme**:**

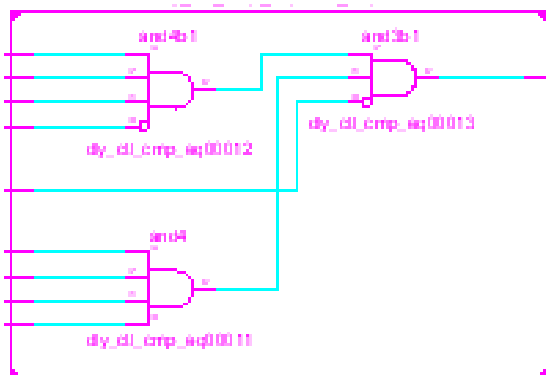


FIGURE 4: VLSI architecture developed for fixed point for different stages of butterfly

The above figure illustrates that the output samples of the FFT .In FFT the bits should be reversed and also we need to calculate the twiddle factor. The reordering scheme starts depending on the index value .Utilizing the different band intervals in the multicarrier architectures, this altering design can achieve the corresponding result samples of 512-point FFT in reverse bit order.

$$W_N = e^{-J\frac{2\pi}{N}}, \text{twiddle factor}$$

$$X_k = \sum_{i=0}^{N-1} x_i W_N^{ki}, 0 \le k < N$$

$$x_i = \sum_{k=0}^{N-1} x_k W_N^{-ki}, \ 0 \le k < N$$

Where, " i " represents sample indication and
K is the subcarrier indication

4.4 Converting Simulink Blocks to HDL Synthesis

In this we have designed the 512 point in MATLAB software and directly we are converting the Simulink block figure into HDL synthesis. It is an easy approach to delay and we can easily calculate the no of clock cycles. These results can be shown in chapter 5.

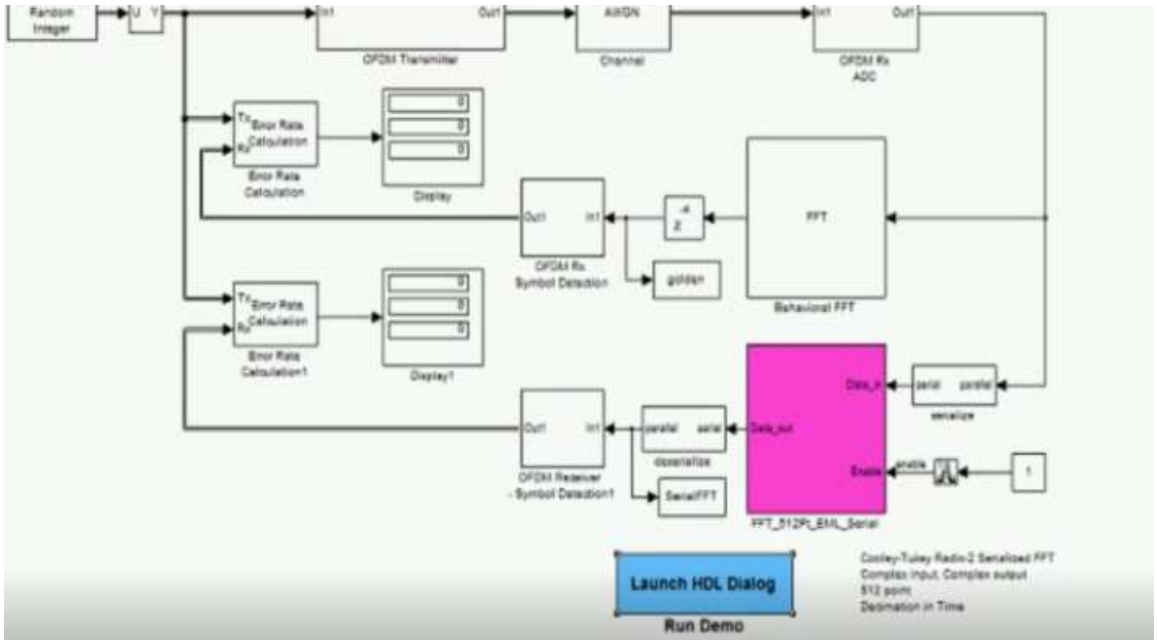


Figure 5: MATLAB Simulink block

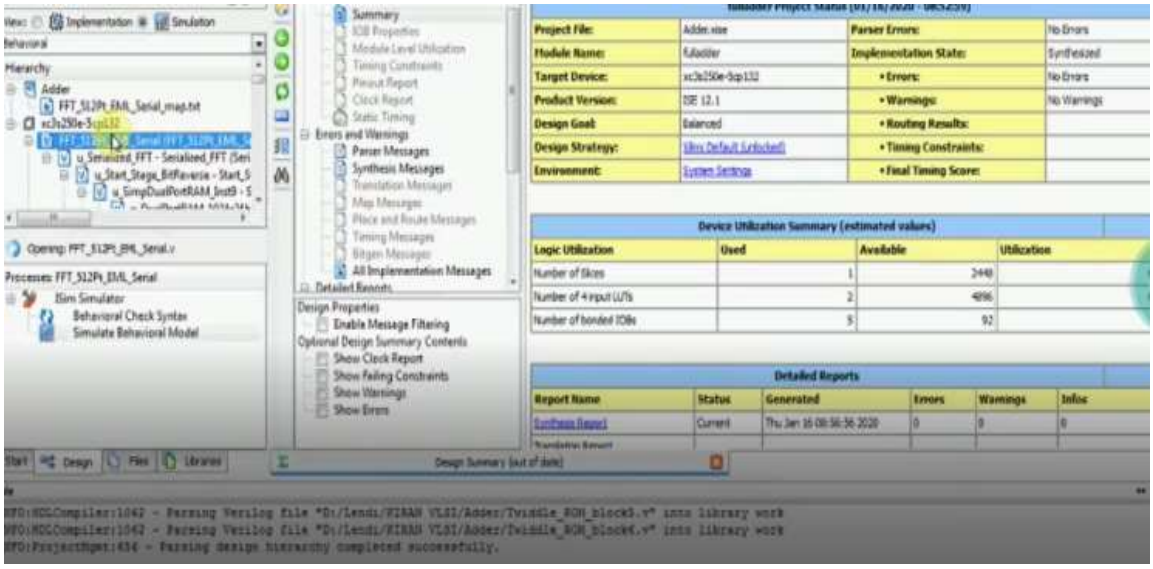
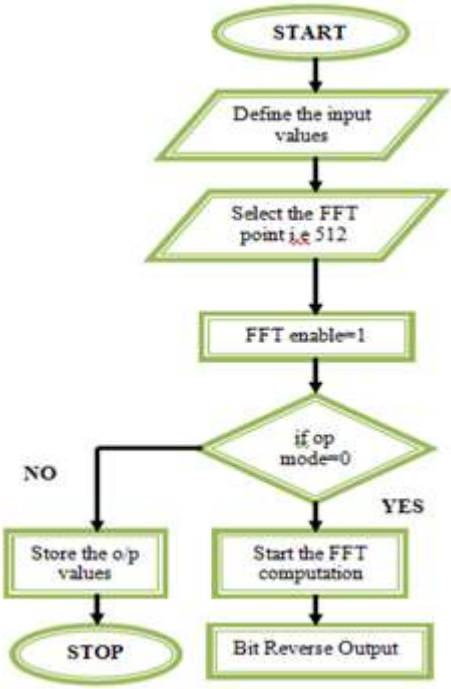


Figure 6: HDL Conversion

4.5 Cooley–Tukey FFT algorithm

To execute the FFT there are many algorithms that we have used the "Cooley–Tukey FFT" algorithm. We have been using this algorithm because it is the fastest algorithm and no of computations can also be easily reduced .We have written a logic based on this algorithm in verilog style. Basically it computes the size of an FFT and also to reduce the processing time.For suppose there are two lengths N1 and N2 of an array they are multiplied with twiddle factor and after multiplying we should find N1 and N2 to get the final result. The order of the Cooley Tukey algorithm no of additions and multiplications for all of them the order is NlogN .Because the speed and execution time of the FFT depends on the algorithm .And the logic rely on size of the FFT point .Take an example if there is 8 point it should have 3 butterfly stages. The algorithm uses the periodic properties of the sine and cosine function to implement the butterflies and there are so many algorithms we have used this algorithm because its complexity is less then compared to other algorithms.

4.6 Flow chart of FFT:



Algorithm of FFT:

Step 1: Start the implementation.
Step 2: Give the input values
Step 3: Select the point of the FFT and for which you are designing.
Step 4: To compute the FFT the fft enable value should always equal to 1
Step 5: Take a condition that if operating mode value is 0 if this condition is true then start the FFT computation otherwise store the outputs.
Step 6: If it is true the output must be bit reversed otherwise stop the execution.

V. OBSERVATIONS AND RESULTS

Designing the variable stages of butterfly figure and we know that for every 2^n points there are n stages .Below figure shows that designing of 512- point FFT as there are 9 stages.

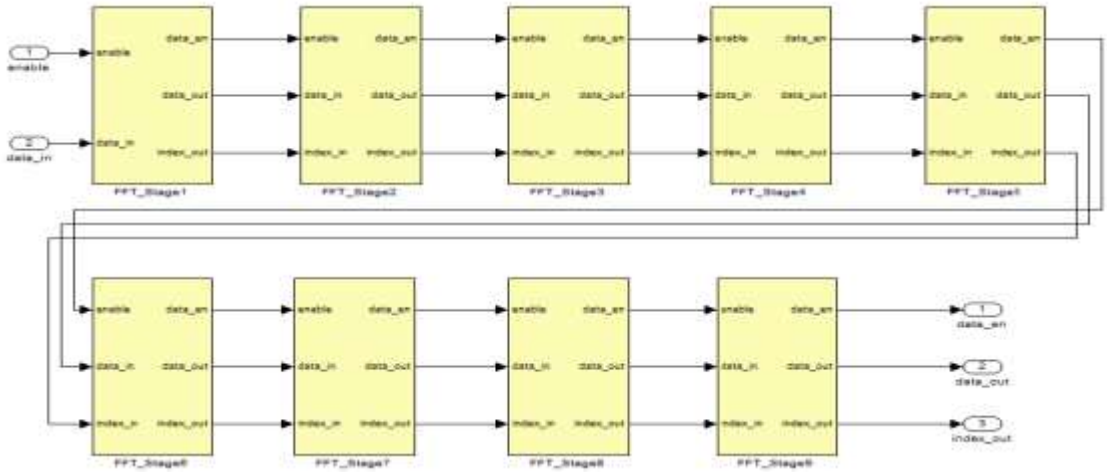


Figure 8: FFT 512 point 9-STAGES

Now we have implemented the 512 point and the corresponding latency calculation ,designing and the RTL schematic is shown in below figures.

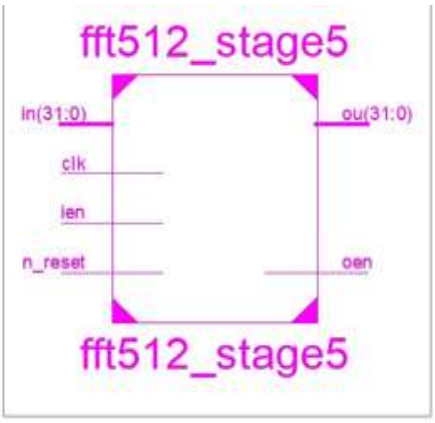


Figure 9: 512 Point FFT

In the below figure there 9 butterfly stages for each and every stage is designed and finally we got the results as shown below

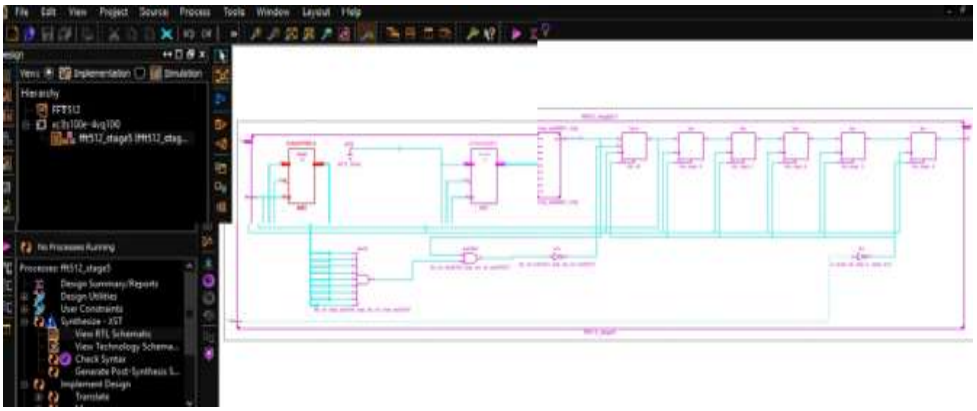


Figure 10: RTL Schematic of 512-Pt FFT

To calculated the time delay as shown in the below figure it is in nanoseconds,

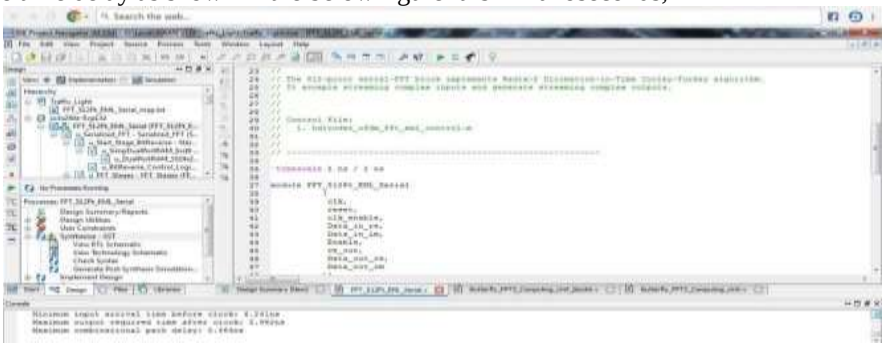


Figure 11: Latency calculation

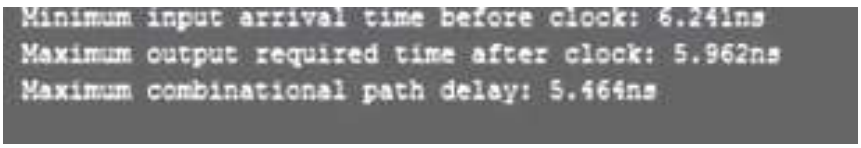


Figure 12: No of clock cycles

The timing diagram is also shown below

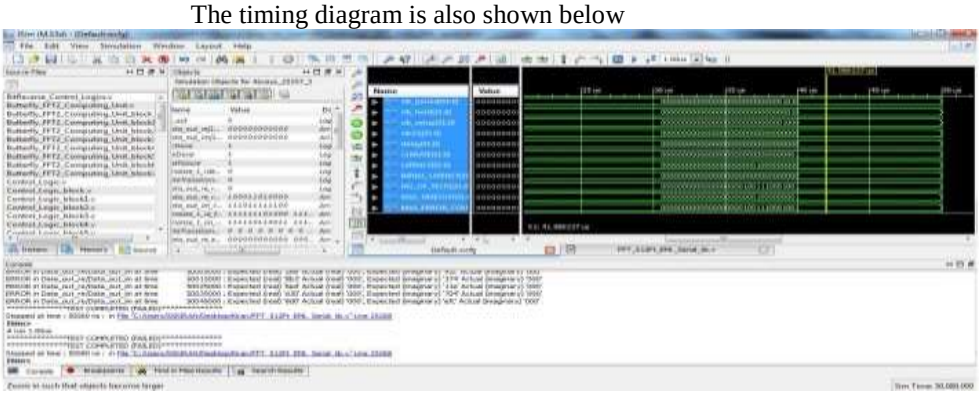


Figure 13: Timing diagram of 512 point

V1. CONCLUSION AND APPLICATIONS

In this paper, we have proposed the 512 point FFT for massive MIMO utilizing the chip routing technology for 512 point we have calculated the latency which shows in nanoseconds and no of computations and time delay, clock cycles are reduced. And also in this proposed system we have implemented this idea in VLSI and MATLAB software and this FFT is used in the communication for good transmission and receiving.

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