DESIGN OF LOW POWER FULL ADDER USING ADIABATIC LOGIC

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ABSTRACT
VLSI technology permits the designers to put additional variety of gates in a single IC. so a to realize the moveable VLSI primarily based application circuits the action of power optimization is important. In planning the complicated circuits like multipliers, dividers, modulators, the total adder could be a basic useful component in them. so as to get overall power improvement during a VLSI IC, the most aim is to cut back the facility consumption of the total adder. to style associate economical one bit full adder that is energy economical we have a tendency to are mistreatment the adiabatic logic here. The result of mistreatment the adiabatic logic is it neglects the quantity of exchange of energy with the encompassing atmosphere. Therefore the circuits that are designed mistreatment this logic can have negligible energy loss because of cooling. In VLSI, there's got to contemplate space, power and delay to supply {an effective an economical a good} and efficient full adder circuit. to beat all those issues during this project. we are mistreatment ALFA(Adiabatic Logic primarily based Full Adder) cell style approach during which by mistreatment eighteen transistors we are able to cut back the facility consumption.

Keywords: Adiabatic logic, pass transistor logic, energy dissipation, Adiabatic Switching.

INTRODUCTION

VLSI (Very Large Scale Integration) is that the method of making Associate in Nursing microcircuit combining thousands of transistors into one chip. Reducing power consumption full adder circuits is crucial for VLSI primarily based circuits. Most of those application circuits incorporate processor-based blocks. Principally those circuits can have Full adder as their main part. Hence, so as to get the power improvement in an exceedingly VLSI IC, as Associate in Nursing initial try, the facility reduction fully adders is that the prime aim of the VLSI designers. Thus, so as to own Associate in Nursing economical approach, that's to implement the applying circuits within the VLSI. IC give several selections for describing, synthesizing and confirmatory the styles with reduced complexness. Depletion of the semiconductor space throughout fabrication results in the decline in power consumption. Thus, selecting low power overwhelming logic designs within the logical style stage and up the potency of the physical style stage by adopting increased placement and routing techniques can yield a coffee power style with reduced propagation delay. With this perception, the planning and implementation of a coffee power full adder cell were distributed by choosing the low power overwhelming logic designs like CMOS primarily based 28T full adder cell, PTL primarily based 16T full adder cell with TG, PTL primarily based 14T full adder cell with TG and planned ALFA cell. In VLSI, there's a trade-off between space, power and delay. to beat these problems, it's

needed {to style to style} Associate in Nursing optimized design. thus the ALFA cell is planned to beat the issues of the prevailing techniques like CMOS Full Adder, PTL logic and transmission gate. The flow of this paper represented full adder victimization varied logic designs, elaborates the less space occupying and low power overwhelming economical ALFA cell style approaches, the simulation outputs of the designed full adder cells with the thought of logic designs square measure illustrated along side their individual space and power consumption results.

Basic full adder design

Full Adder is that the adder that adds 3 inputs and produces add and carry as outputs. the primary 2 inputs area unit A AND B and also the third input is an input carry as C-IN. The output carry is selected as C-OUT and also the traditional output is selected as S which is SUM. Full adder logic is intended in such a way which will take eight inputs along to form a byte-wide adder and cascade the carry bit from one adder to another.

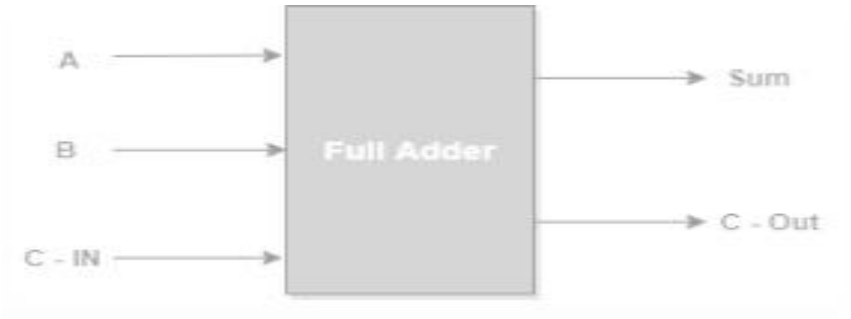

Figure 1: Basic Full adder block diagram

Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Full Adder Truth Table

Logical Expression for SUM:

= A’ B’ C-IN + A’ B C-IN’ + A B’ C-IN’ + A B C-IN

= C-IN (A’ B’ + A B) + C-IN’ (A’ B + A B’)

= C-IN XOR (A XOR B)= (1,2,4,7)

Logical Expression for C-OUT:

= A' B C-IN + A B' C-IN + A B C-IN' + A B C-IN

= A B + B C-IN + A C-IN= (3,5,6,7)

Another form in which C-OUT can be implemented:

= A B + A C-IN + B C-IN (A + A')

= A B C-IN + A B + A C-IN + A' B C-IN

= A B (1 +C-IN) + A C-IN + A' B C-IN

= A B + A C-IN + A' B C-IN

= A B + A C-IN (B + B') + A' B C-IN

= A B C-IN + A B + A B' C-IN + A' B C-IN

= A B (C-IN + 1) + A B' C-IN + A' B C-IN

= A B + A B' C-IN + A' B C-IN

= AB + C-IN (A' B + A B')

Therefore COUT = AB + C-IN (A EX – ORB)

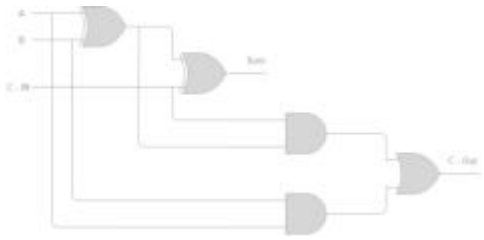

Figure 2: Full Adder logic circuit

Pass semiconductor logic related to transmission gates Transmission gates are the absolutely restoring logic version of PTL whose output logic level doesn't degrade once passed through the individual logic level signal offered on its inputs. Hence, in coming up with the total adder cells with PTL, so as to induce the non- degraded outputs of the total and carry, transmission gates are befittingly inserted into the designs. PTL with TG based 16T full adder cell PTL with TG based mostly 16 transistors full adder cell is shown in Fig. 2.The simulation results show that the PTL with TG based mostly 16T full adder cell has lower power consumption than that of the CMOS based 28T full adder cell. The PTL with TG based mostly fourteen transistors full adder cell is shown in Fig. 3.It has lower dynamic power consumption in comparison to the CMOS based 28T full adder cell. A Simple adiabatic computer circuit In this we are going to examine straightforward circuit configurations that can be used for adiabatic switching. A general circuit topology for the

conventional CMOS gates and adiabatic counterparts is shown in Figure3. To convert a conventional CMOS logic gate into an adiabatic gate, the pull-up transistor and the pull-down semiconductor unit networks should get replaced with complementary transmission-gate(T-gate).The T-gate network implementing the pull-up perform is employed to drive truth output of the adiabatic gate, whereas the T-gate network implementing the pull down perform drives the complementary output node.

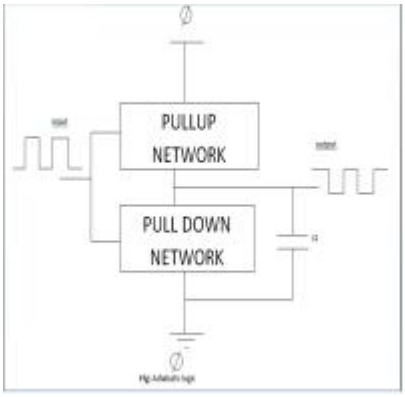

Figure 3: A Simple Adiabatic Logic Gate

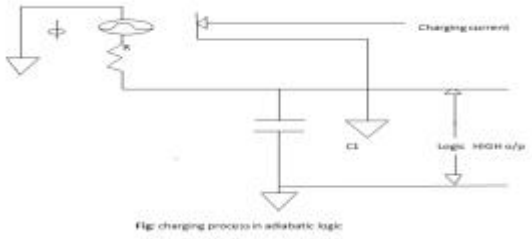

Figure 4: An Adiabatic Logic Gate showing Charging Path

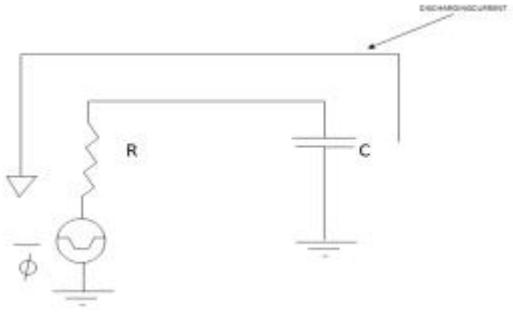

Figure 5: associate degree adiabatic gate Showing Discharging Path

Note that each one the inputs ought to even be obtainable in complementary type. Both the pull-up and pull-down networks within the adiabatic logic circuit are used for charging in addition as discharging the output node capacitance, which ensures that the energy stored at the output node may be retrieved by the ability offer, at the tip of every cycle shown in Figure four. to permit adiabatic operation, the DC voltage source of the original circuit must be replaced by a variable power offer with the ramped voltage output. The necessary circuit modifications that are accustomed convert a standard CMOS logic circuit into associate degree adiabatic logic circuit increase the device count by an element of 2 or perhaps a lot of.

ADIABATIC LOGIC FAMILIES:

Adiabatic logic circuits classified into 2 types:

(a) Quasi/ Partial adiabatic Logic Circuits (b)Full adiabatic Logic Circuits

a) Quasi/Partial adiabatic Logic Circuits: Quasi- adiabatic circuits have straightforward design and power clock system. The adiabatic loss happens once current flows through non-ideal switch, which is proportional to the frequency of the power-clock. Popular partly adiabatic families embrace the following:

(i)True Single-Phase adiabatic Logic(TSEL). (ii) Source-coupled adiabatic Logic(SCAL).

b) Full adiabatic Logic Circuits:
Full-adiabatic circuits haven't any non-adiabatic loss, however they're way more complicated than quasi-adiabatic circuits. All the charge on the load capacitance is recovered by the ability offer. totally adiabatic circuits face heaps of issues with relation to the operational speed and the inputs power clock synchronization.

Some totally adiabatic logic families include:

(i) Efficient Charge Recovery Logic (ECRL).
(ii) 2N-2N2P Adiabatic Logic.
(iii) Positive Feedback adiabatic Logic (PFAL).
(iv) Pass electronic transistor adiabatic Logic(PAL).
(v) Split-Rail Charge Recovery Logic (SCRL).

NMOS Energy Recovery Logic (NERL):

NMOS energy recovery logic (NERL), that uses NMOS transistors only and a simpler 6-phase clocked power. Its area over head and energy consumption square measure smaller, compared

with the opposite absolutely adiabatic logics. we have a tendency to utilized bootstrapped NMOS switches to alter the NERL circuits. With the simulation results for a full adder, we have a tendency to confirmed that the NERL circuit consumed well less energy than the opposite adiabatic logic circuits at low-speed operation. NERL is additional appropriate than the opposite adiabatic logic circuits for the applications that don't need high performance however low energy consumption.

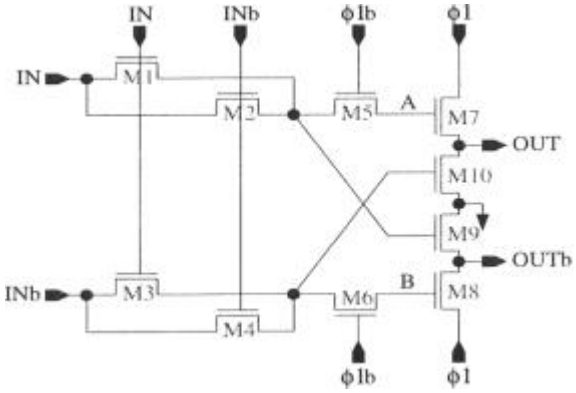

Figure 6: NMOS energy recovery logic gate

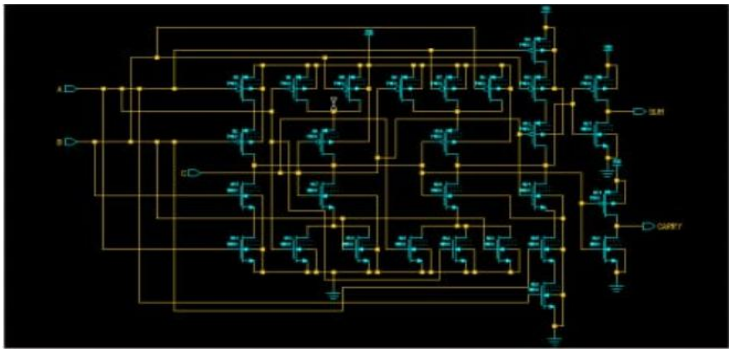

Figure 7: Basic full adder circuit(28T)

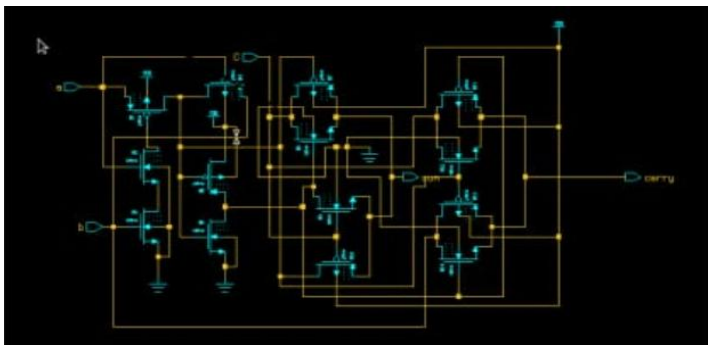

Figure 8:14T full adder circuit

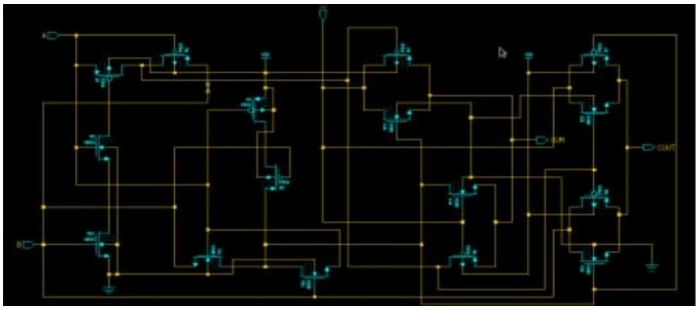

Figure 9:16T full adder circuit

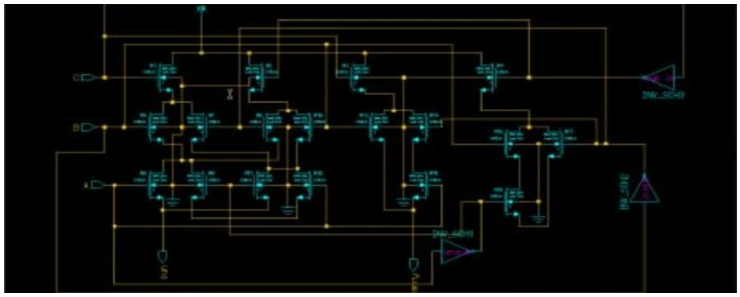

Figure 10:18T full adder circuit

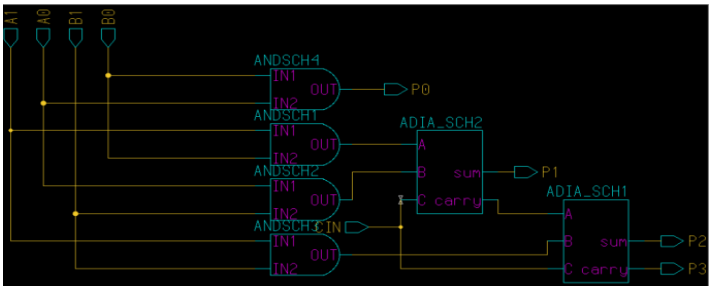

Figure 11: Multiplier 2x2 circuit

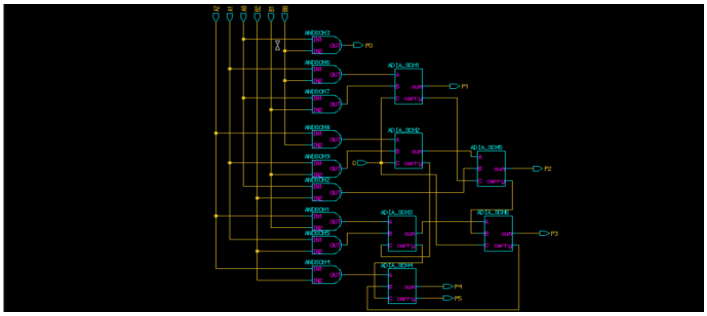

Figure 12: Multiplier 3x3 circuit

Simulation results

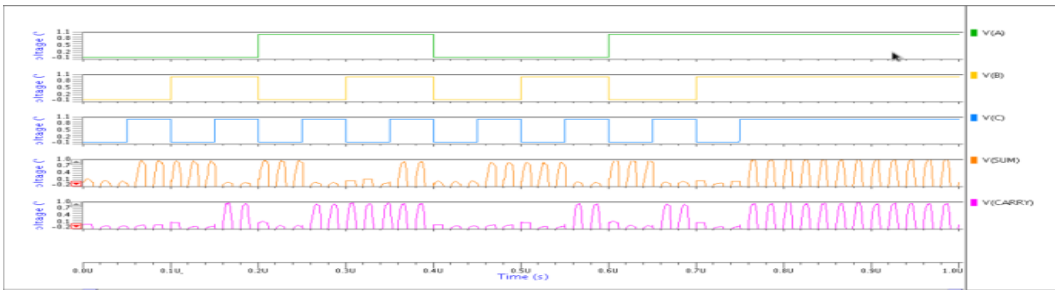

Figure 13: Simulation of 18T ALFA cell

Figure illustrate the simulation output of the proposed ALFA cell. The outputs are represented as a sum, carryout, inverted sum and inverted Carry out.

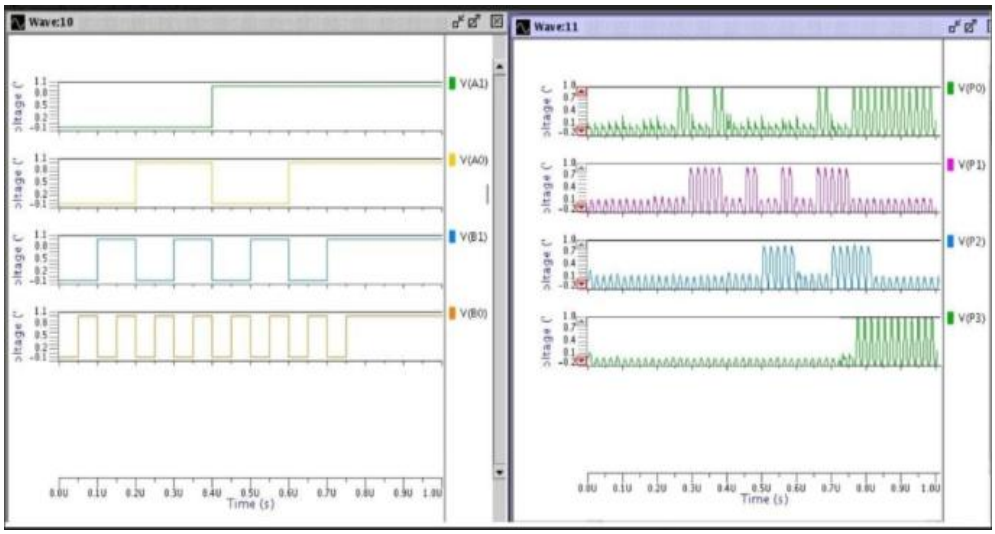

Figure 14: Simulation of 2x2 Multiplier

A 2x2 Multiplier is a circuit which takes 2 inputs as 2 bits and it will perform the multiplication of that as shown in the output Figure14.

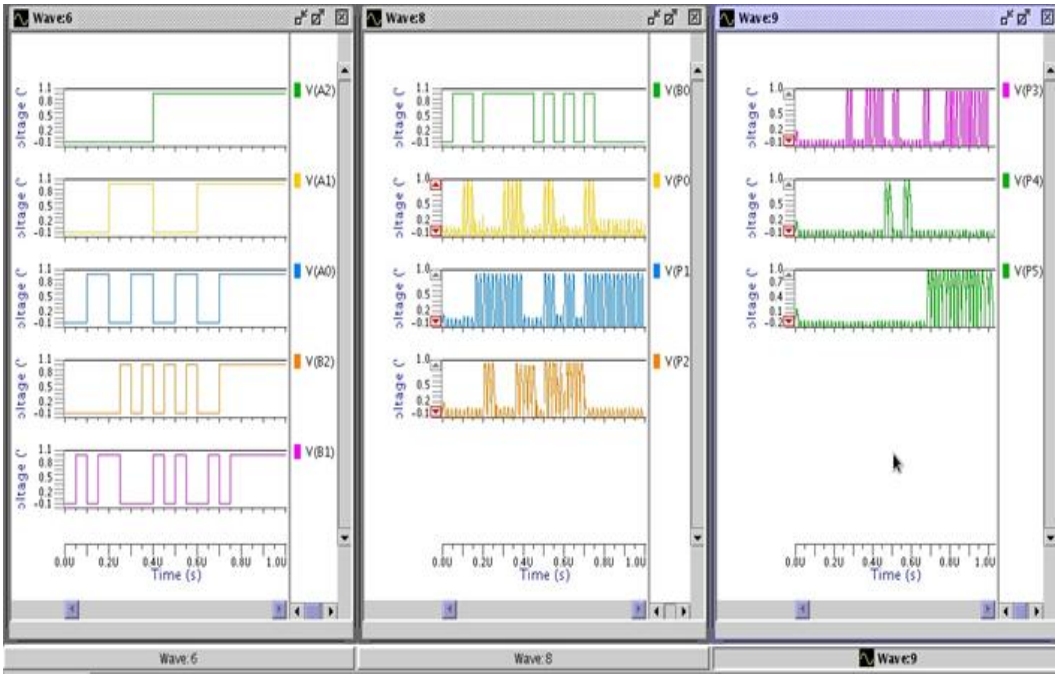

Figure 15: Simulation of 3x3 Multiplier

A 3x3 Multiplier is a circuit which takes 3 inputs as 3 bits and it will perform the multiplication of that as shown in the output Figure15.

S.No	Full Adder Design	Power (nW)
1	28T Full adder	4.4613
2	16T PTL and TG	3.5195
3	14T PTL and TG	7.0155
4	18T Adiabatic Full Adder Logic	2.296

Table 2: Power analysis of various full adder logic styles

CONCLUSION

The ALFA cell has lower power consumption than that of the opposite versions of the complete adder cell attributable to energy exercise. Associate ultra-power optimized ALFA cell is planned victimization adiabatic logic with the help of lower activity space. The performance analysis of full adders in several logic designs is dispensed with the main target on getting optimized power consumption.

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